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ABSTRACT:

PROBLEM TO BE SOLVED: To generate a read/write address to a memory so that a continuous interleaving processing on data of a plurality of blocks is realized with one memory.

SOLUTION: An address generator 1 generating a read/write address to a memory for executing an interleaving on N rows  $\times$  M columns where N $\times$ M data are made into one block is provided with an address counter 3 executing count-up from zero at step width which is synchronized with a clock and is

inputted, outputting the count value as the address,  
setting a value obtained  
by modulo-operating the value by  $(N \times M - 1)$  to be the  
next count value when  
the count value at the next clock becomes not less than  
 $(N \times M)$ , and  
returning the next count value to '0' when the count value  
becomes  
 $(N \times M - 1)$  and a step width computing element 5 changing  
step width to the  
counter 3 to a value obtained by  $(N \times M - 1)$   
modulo-operating a value obtained  
by multiplying step width till then by M whenever the count  
value returns to  
'0'.

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# PATENT ABSTRACTS OF JAPAN

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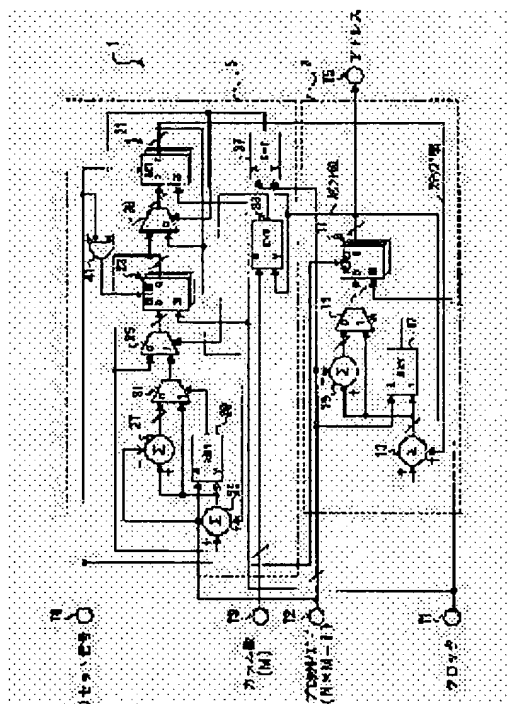
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## (54) INTERLEAVING ADDRESS GENERATOR AND INTERLEAVING ADDRESS GENERATION METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To generate a read/write address to a memory so that a continuous interleaving processing on data of a plurality of blocks is realized with one memory.

SOLUTION: An address generator 1 generating a read/write address to a memory for executing an interleaving on  $N$  rows  $\times$   $M$  columns where  $N \times M$  data are made into one block is provided with an address counter 3 executing count-up from zero at step width which is synchronized with a clock and is inputted, outputting the count value as the address, setting a value obtained by modulo-operating the value by  $(N \times M - 1)$  to be the next count value when the count value at the next clock becomes not less than  $(N \times M)$ , and returning the next count value to '0' when the count value becomes  $(N \times M - 1)$  and a step width computing element 5 changing step width to the counter 3 to a value obtained by  $(N \times M - 1)$  modulo-operating a value obtained by multiplying step width till then by  $M$  whenever the count value returns to '0'.



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**DETAILED DESCRIPTION**

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the interleave processing for reducing the effect of the burst error in a digital communication system about a digital-communication technique.

[0002]

[Description of the Prior Art] Generally, big effectiveness is not acquired even if it applies the error correction processing by the Viterbi decoder, the Lead Solomon decoder, etc. directly to the data transmitted on a radio-transmission way, since error data generate intensively the burst error generated in the radio-transmission on the street of a digital communication system.

[0003] Then, the concentrated error data based on an burst error are distributed, and he changes into a random error, and is trying for this to aim at an improvement of the error correction effectiveness by using interleave processing together with error correction processing to the data transmitted on a radio-transmission way conventionally.

[0004] He replaces the sequence of data and is trying to transmit by the transmitting side in this interleave processing. And data are returned in order of origin by performing actuation contrary to a transmitting side by the receiving side. Since the burst error in a transmission line is distributed and it is changed into a random error by carrying out like this, the error correction effectiveness can be heightened.

[0005] Here, in such interleave processing, in order to replace the sequence of the data which make 1 block  $N \times M$  piece (however,  $M$  [  $N$  and ] 2 or more integers), there is a method of using RAM (random access memory). and he performs X-Y conversion with an imagination line address and the train address, and is trying to output input data in different sequence from the sequence at the time of an input by this approach by writing input data in RAM in order of that line address, assuming that it is what has the line address of  $N$  line, and the train address of  $M$  train in RAM, and reading data from RAM in order of the train address after that write-in termination

[0006] As shown in drawing 7, for example, the conventional interleave circuit 101 which performs such interleave processing RAM103 which outputs the stored data from the data output terminal DOUT while storing the input data from the data input terminal DIN, the  $n+1$ -bit address counter 105 which performs count-up actuation every [ 1 ] from initial value 0 synchronizing with the clock from the clock input terminal CLK -- and  $n+1$ -bit data  $Q_0 - Q_n$  outputted from an address counter 105 In inside the most significant bit  $Q_n$   $n$  bit-data  $Q_0 - Q_{n-1}$  of an except the 1st for  $n$  bits -- input terminal  $a_0 - a_{n-1}$  While being inputted above-mentioned  $n$  bit-data  $Q_0 - Q_{n-1}$  from an address counter 105 Low order  $m$  bit  $Q_0 - Q_{m-1}$  which can be set High order  $(n-m)$  bit  $Q_m - Q_{n-1}$   $n$  bit-data  $Q_m - Q_{n-1}$  replaced and  $Q_0 - Q_{m-1}$  the 2nd for  $n$  bits -- input terminal  $b_0 - b_{n-1}$  It has the interleave address generation machine which consists of an inputted address selector 107.

[0007] And an address selector 107 is the most significant bit  $Q_n$  of an address counter 105. For example, in being "0" the 1st -- input terminal  $a_0 - a_{n-1}$  Data  $Q_0 - Q_{n-1}$  from the address counter 105 inputted output terminal  $Y_0 - Y_{n-1}$  of self from -- address input terminal  $A_0 - A_{n-1}$  of RAM103 Write in

and it outputs as the address. On the contrary, the most significant bit  $Q_n$  of an address counter 105 In being "1" the 2nd -- input terminal  $b_0 - b_{n-1}$  Data  $Q_m - Q_n - 1$  from the address counter 105 inputted, and  $Q_0 - Q_{m-1}$  Output terminal  $Y_0 - Y_{n-1}$  of self from -- address input terminal  $A_0 - A_{n-1}$  of RAM103 It reads and outputs as the address.

[0008] And RAM103 is the most significant bit  $Q_n$  of an address counter 105 further. In being "0" The data by which a sequential input is carried out from the data input terminal DIN synchronizing with a clock Address input terminal  $A_0 - A_{n-1}$  It stores in the address shown with the data inputted, and is the most significant bit  $Q_n$  of an address counter 105. In being "1" Address input terminal  $A_0 - A_{n-1}$  Synchronizing with a clock, the sequential output of the data of the address shown with the data inputted is carried out from the data output terminal DOUT.

[0009] When writing input data in RAM103 in such an interleave circuit 101, it is  $n$  bit-data  $Q_0 - Q_{n-1}$  from an address counter 105 by the address selector 107. It is address input terminal  $A_0 - A_{n-1}$  of RAM103 as it is. Since it writes in and is outputted as the address, data will be written in sequentially from the 0th street of RAM103.

[0010] moreover, in reading data from RAM103 an address selector 107 --  $n$  bit-data  $Q_0 - Q_{n-1}$  from an address counter 105 Low order  $m$  bit  $Q_0 - Q_{m-1}$  which can be set High order  $(n-m)$  bit  $Q_m - Q_{n-1}$   $n$  bit-data  $Q_m - Q_{n-1}$  replaced and  $Q_0 - Q_{m-1}$  Address input terminal  $A_0 - A_{n-1}$  of RAM103 Since it reads and is outputted as the address, data will be read in the sequence which replaced the line address and the train address of RAM103 to the time of the writing of data.

[0011] For example, when interleave processing in four line  $x4$  train is performed, the input data from the data input terminal DIN will be written in RAM103 in order of the address shown in drawing 8 (A) (namely, when interleave processing is performed having used  $4x4$  data as 1 block). And when all the data of 16 (=  $4x4$ ) individual for 1 block are written in next, data will be read from RAM103 in order of the address shown in drawing 8 (B), and the sequential output of the read data will be carried out from the data output terminal DOUT. In addition, the number in O in drawing 8 (A) shows the sequence of the address which writes in data, and the number in \*\* in drawing 8 (B) shows the sequence of the address which reads data.

[0012] Therefore, supposing it attaches D1, D2 and D3, --, an index called D14, D15, and D16 sequentially from the 1st thing to the input data for 1 block From the data output terminal DOUT, input data will be rearranged and outputted to D1, D5, D9, D13 and D2, D6, D10, D14 and D3, D7, D11, D15 and D4, D8, and order called D12 and D16.

[0013]

[Problem(s) to be Solved by the Invention] By the way, in the above-mentioned conventional interleave circuit 101, it is necessary to hold the data for 1 block until it finishes data read-out from RAM103. therefore, in order to carry out interleave processing of the data of two or more blocks by which a sequential input is carried out continuously Two circuit blocks 101A and 101B which have the same configuration as the interleave circuit 101 of drawing 7 as shown in drawing 9, The delay circuit 109 which delays by 1 block that a clock begins to be supplied to one circuit block 101B, The most significant bit  $Q_n$  of the address counter 105 in circuit block 101A of another side When it is "1" The data outputted from the data output terminal DOUT of circuit block 101A are outputted as output data, and it is the above-mentioned most significant bit  $Q_n$  conversely. In being "0" From the selector 111 outputted as output data, the data outputted from the data output terminal DOUT of circuit block 101B An interleave circuit is constituted and it is necessary to make it each of the circuit blocks 101A and 101B take charge of the phase which writes data in RAM103, and the phase which reads data from RAM103 by turns to timing as shown in drawing 10.

[0014] In addition, drawing 10 shows the case where interleave processing is performed having used  $4x4$  data as 1 block, like drawing 8. And it sets to drawing 10 and is  $Q_n$ . For the output data to 1-16, and a number, interleave processing is carried out by circuit block 101A, and the number currently outputted when it is "1" is [ 33 or more output data ]  $Q_n$ . When it is "0", as for the output data to 17-32, interleave processing of the number currently outputted is carried out by circuit block 101B.

[0015] Thus, in the Prior art, in order to perform interleave processing continuously to the data of two or

more blocks by which a sequential input is carried out, it was difficult to miniaturize the circuit for forming the interleave address generation machine which consists of an address counter 105 and an address selector 107, and every two RAM103, and performing interleave processing. And since especially interleave processing of this kind is carried out with mobile communication equipment etc., it is required that the circuit which performs interleave processing should be small.

[0016] Then, this invention aims at offering the interleave address generation machine and the interleave address generation approach of carrying out continuous interleave processing to the data of two or more blocks by one memory.

[0017]

[The means for solving a technical problem and an effect of the invention] The interleave address generation approach of this invention made in order to attain the above-mentioned purpose While carrying out the sequential input of the data according to claim 4 which make 1 block a  $N \times M$  individual (however,  $M \geq N$  and  $N \geq 2$  or more integers) like and writing in memory By reading in order of the address which writes in the data written in the memory and is different from the time It is used in order to perform interleave processing which outputs the inputted data in different sequence from the sequence at the time of an input, and read-out in said memory and the address for writing are generated.

[0018] And the interleave address generation approach of this invention While performing count-up from initial value 0 with the set-up step size and carrying out the sequential output of the counted value as read-out in said memory, and the address for writing When the following counted value becomes beyond the above ( $N \times M$ ) When it considers as the following counted value and further this counted value becomes ( $N \times M - 1$ ), the value which took the modulo of ( $N \times M - 1$ ) about the value Address count processing in which the following counted value was returned to initial value 0, It consists of step size setting processing in which said step size used by this address count processing is set up. In step size setting processing The value which took the modulo of ( $N \times M - 1$ ) about the value which multiplied the step size which is carrying out a current setup by said  $M$  Ask as a new step size at the time of the interleave processing to the following block, and it synchronizes with the timing from which the counted value by said address count processing returned to initial value 0. It is characterized by updating the step size used by said address count processing to said new step size for which it asked.

[0019] Moreover, such an interleave address generation approach of this invention can be enforced with an interleave address generation vessel according to claim 1. Namely, an interleave address generation circuit according to claim 1 While carrying out the sequential input of the data which make 1 block a  $N \times M$  individual (however,  $M \geq N$  and  $N \geq 2$  or more integers) and writing in memory By reading in order of the address which writes in the data written in the memory and is different from the time It is used in order to perform interleave processing which outputs the inputted data in different sequence from the sequence at the time of an input, and read-out in said memory and the address for writing are generated, and it has the address count means and the step size operation means.

[0020] And count-up actuation is performed from initial value 0 with the step size which an address count means synchronizes with a clock, and is inputted from the exterior. While outputting the counted value as read-out in said memory, and the address for writing, when the counted value in the following clock timing becomes beyond the above ( $N \times M$ ) When the value which took the modulo of ( $N \times M - 1$ ) about the value is made into the counted value in the following clock timing and further this counted value becomes ( $N \times M - 1$ ), it is constituted so that the counted value in the following clock timing may be returned to initial value 0.

[0021] And further, although a step size operation means calculates the step size used for count-up actuation and an address count means outputs it to said address count means The value which took the modulo of ( $N \times M - 1$ ) especially about the value which multiplied the step size which is carrying out the current output by said  $M$  It sets up as a new step size at the time of the interleave processing to the following block, and the step size outputted to said address count means is changed into said set-up new step size synchronizing with the timing from which the counted value of said address count means returned to initial value 0.

[0022] In addition, the step size means the value of the increment in every time at the time of counting

up the counted value used as the address to memory. Moreover, the value which took the modulo of  $(NxM - 1)$  about a certain value  $Z$  means too much value at the time of breaking a certain value  $Z$  by  $(NxM - 1)$ .

[0023] in the interleave address generation approach and interleave address generation machine of such this invention, it will come out and there will be a step size of the address outputted by address count processing or the address count means, whenever the address outputted returns from  $(NxM - 1)$  to initial value 0, and it will be changed for every 1 block of input data.

[0024] Therefore, according to the interleave address generation approach and interleave address generation machine of this invention, it sets at the period which inputs the data of the 1st block (namely, beginning). Input data to each address of the memory outputted by address count processing or the address count means Sequential writing, In the period which inputs the data of each block of the 2nd henceforth While reading data from each address of the memory outputted by address count processing or the address count means By overwriting current input data to the read address, addressing of the read-out of the data from memory will be carried out with a different step size from the time of writing in the data. For this reason, the continuous interleave processing to the data of two or more blocks is attained only by having memory and an interleave address generation machine 1 set.

[0025] For example, while setting initial value of a step size to 1, the case where interleave processing is performed with a block size with a line count (low number)  $N = 4$  and  $M = 3$  trains (the number of columns) is explained concretely (namely, when performing interleave processing in four line x3 train which made 4x3 data 1 block).

[0026] In this case, as shown in the 5th step and the bottom from on drawing 4, in the period which inputs the data (D 1-1 - D 1-12) of the 1st block, the address will be outputted from address count processing or an address count means in order of 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11.

[0027] And it sets at the period which inputs the data (D 2-1 - D 2-12) of the 2nd block, and the step size set up or outputted by step size setting processing or the step size operation means serves as a value (= 3) which took the modulo of 11 ( $=NxM - 1$ ) about the value (= 3) which multiplied the step size (= 1) in the input period of the 1st block by  $M (= 3)$ . Therefore, from address count processing or an address count means, the address will be outputted in order of 0, 3, 6, 9, 1, 4, 7, 10, 2, 5, 8, and 11. In addition, since the value (= 12) which added 3 which is a current step size to 9 becomes more than 12 ( $=NxM$ ) that is the number of data of 1 block, the address outputted is changing to the degree of 9 1 because 1 which is the value which took the modulo of 11 ( $=NxM - 1$ ) about 12 in this case becomes the following counted value. Moreover, since the value (= 13) to which that the address outputted is changing to the degree of 10 similarly 2 also added 3 which is a current step size to 10 becomes more than 12 ( $=NxM$ ), 2 which is the value which took the modulo of 11 ( $=NxM - 1$ ) about 13 in this case is because it becomes the following counted value.

[0028] And it sets further at the period which inputs the data (D 3-1 - D 3-12) of the 3rd block, and the step size set up or outputted by step size setting processing or the step size operation means serves as a value (= 9) which took the modulo of 11 ( $=NxM - 1$ ) about the value (= 9) which multiplied the step size (= 3) in the input period of the 2nd block by  $M (= 3)$ . Therefore, from address count processing or an address count means, the address will be outputted in order of 0, 9, 7, 5, 3, 1, 10, 8, 6, 4, 2, and 11. In addition, since the value (= 18) which added 9 which is a current step size to 9 becomes more than 12 ( $=NxM$ ) that is the number of data of 1 block, the address outputted is changing to the degree of 9 7 because 7 which is the value which took the modulo of 11 ( $=NxM - 1$ ) about 18 in this case becomes the following counted value. And this is the same also about the case where the address outputted changes to the degree of 7 5, and the case where it changes to the degree of 5 3.

[0029] Moreover, although not shown in drawing 4, it sets at the period which inputs the data of the 4th block, and the step size set up or outputted by step size setting processing or the step size operation means serves as a value (= 5) which took the modulo of 11 ( $=NxM - 1$ ) about the value (= 27) which multiplied the step size (= 9) in the input period of the 3rd block by  $M (= 3)$ . Therefore, from address count processing or an address count means, the address will be outputted in order of 0, 5, 10, 4, 9, 3, 8, 2, 7, 1, 6, and 11. In addition, since the value (= 15) which added 5 which is a current step size to 10

becomes more than 12 ( $= NxM$ ) that is the number of data of 1 block, the address outputted is changing to the degree of 10 4 because 4 which is the value which took the modulo of 11 ( $= NxM - 1$ ) about 15 in this case becomes the following counted value. And this is the same also about the case where the address outputted changes to the degree of 9 3, and the case where it changes to the degree of 8 2.

[0030] Therefore, if the data of the 1st block are written in each address of the memory outputted by address count processing or the address count means one by one, each data of the 1st block will be written in the addresses from 0 to 11 of memory in order of the number shown in O of drawing 1 (A).

[0031] And while reading data from each address of the memory outputted by address count processing or the address count means in the period which inputs the data of the 2nd block If current input data is overwritten to the read address, each data of the 1st block already written in memory It is read from the addresses from 0 to 11 in order of the number shown in \*\* of drawing 1 (B). Moreover, each data of the 2nd block It will be written in the addresses from 0 to 11 of memory in order of the number shown in O of drawing 1 (C) (namely, the same sequence as the number shown in \*\* of drawing 1 (B)).

[0032] And further, in the period which inputs the data of the 3rd block, while reading data from each address of the memory outputted by address count processing or the address count means If current input data is overwritten to the read address, each data of the 2nd block already written in memory It is read from the addresses from 0 to 11 in order of the number shown in \*\* of drawing 1 (D). Moreover, each data of the 3rd block It will be written in the addresses from 0 to 11 of memory like the relation between drawing 1 (B) and drawing 1 (C) in order of the number shown in \*\* of drawing 1 (D).

[0033] For this reason, supposing it attaches to order D1, D2, D3, D4, D5, D6, D7, D8, D9, and an index called D10, D11, and D12 from the 1st thing to 12 input data for 1 block The input data of each block by which a sequential input is carried out so that the relation between drawing 1 (A) and drawing 1 (B) and the relation between drawing 1 (C) and drawing 1 (D) may also show By being read from memory, it will be rearranged into the sequence of D1, D4, D7, D10 and D2, D5, D8, D11 and D3, D6, D9, and D12, respectively.

[0034] That is, the interleave processing which continued only by one memory is attained by changing the step size of the address to memory for every 1 block of data with step size setting processing or a step size operation means. In addition, the initial value of a step size is not restricted to 1, and should just be one or more integers. Moreover, what is necessary is to add the address value of the above-mentioned head to the address outputted by address count processing or the address count means, and just to make it supply the address after the addition to the address input terminal of memory, when the number of the start addresses of the memory used for interleave processing is not zero.

[0035] In an interleave address generation machine according to claim 1 by the way, a step size operation means While only said M batch carries out accumulation of the step size according to claim 2 which is carrying out the current output like during the period for [ until the counted value of an address count means serves as ( $NxM - 1$ ) from initial value 0 ] 1 block A step size setting means to set up the value which took the modulo of ( $NxM - 1$ ) about the accumulation value as a new step size at the time of the interleave processing to the following block, A detection means to detect that the counted value of an address count means became ( $NxM - 1$ ), If it is detected that the counted value of an address count means became ( $NxM - 1$ ) with this detection means, while memorizing the new step size set up with said step size setting means to the following clock timing a step size output means to output the memorized this step size to an address count means -- since -- it can constitute.

[0036] That is, with the interleave address generation vessel according to claim 2, the value which multiplied the step size which is carrying out the current output by said M is calculated, when only said M batch carries out accumulation of the current step size. In an interleave address generation machine according to claim 1 moreover, a step size operation means While performing the multiplication of the step size according to claim 3 which is carrying out the current output like and said M A step size setting means to set up the value which took the modulo of ( $NxM - 1$ ) about the multiplication value as a new step size at the time of the interleave processing to the following block, A detection means to detect that the counted value of an address count means became ( $NxM - 1$ ), If it is detected that the counted value of an address count means became ( $NxM - 1$ ) with this detection means, while memorizing the new step

size set up with said step size setting means to the following clock timing a step size output means to output the memorized this step size to an address count means -- since -- it can also constitute.

[0037] That is, with the interleave address generation vessel according to claim 3, the value which multiplied the step size which is carrying out the current output by said M is calculated by carrying out the multiplication of a current step size and said M. However, since the direction constituted so that accumulation of the step size according to claim 2 which is carrying out the current output may be carried out M times like does not need to perform multiplication directly, it is advantageous at the point that circuitry can be simplified.

[0038]

[Embodiment of the Invention] Hereafter, 1 operation gestalt of this invention is explained using a drawing. First, drawing 2 is a block diagram showing the configuration of the interleave address generation machine 1 of the 1st operation gestalt, and drawing 3 is the detailed circuit diagram of the interleave address generation machine 1.

[0039] In addition, the interleave address generation machine 1 of a \*\*\*\* 1 operation gestalt generates read-out in the memory (specifically RAM) which is not illustrated, and the address for writing, in order to perform interleave processing in the N line xM train which made 1 block the data of a NxM individual (however, M[ N and ] 2 or more integers). Moreover, in the following explanation, Above M is called "number of columns" which means the number of trains, and the above (NxM) which is the number of data of 1 block is called "block size."

[0040] As shown in drawing 2, the interleave address generation machine 1 of a \*\*\*\* 1 operation gestalt Count-up actuation is performed from initial value 0 with the step size which synchronizes with a clock from the clock input terminal T1, and is inputted from the exterior. The address counter 3 which outputs the counted value as read-out in memory, and the address for writing, The address outputted from the address counter 3, the data showing the block size -1 ( $= NxM - 1$ ) inputted from the block-size input terminal T2, And based on the data showing the number of columns ( $= M$ ) inputted from number input terminal T3 of columns, it consists of step size computing elements 5 which calculate and output the step size in an address counter 3 synchronizing with the clock from the clock input terminal T1.

[0041] in addition -- an address counter 3 and the step size computing element 5 -- reset-signal input terminal T four -- minding -- a high -- an active reset signal is inputted. Moreover, the data which express the block size -1 ( $= NxM - 1$ ) from the block-size input terminal T2 also with an address counter 3 are inputted. Furthermore, the address is outputted to memory through the address output terminal T5 from an address counter 3.

[0042] As shown in drawing 3, next, an address counter 3 The counted value of the address counter 3 concerned is memorized synchronizing with the clock from the clock input terminal T1. Output the memorized counted value to the address output terminal T5 as the address to memory. The flip-flop group 11 (henceforth the F/F group 11) which consists of a flip-flop with a clock synchronization reset function of the number corresponding to input bus width of face, The adder 13 adding the step size inputted from the output value (namely, address to the memory which is the current counted value of the address counter 3 concerned, and is carrying out the current output) and the step size computing element 5 of the F/F group 11, The subtractor 15 which subtracts the data (only henceforth a block size -1) showing the block size -1 inputted from the block-size input terminal T2 from the result of an operation of the adder 13, The size comparison of the result of an operation of an adder 13 and the block size -1 from the block-size input terminal T2 is carried out. When the result of an operation of an adder 13 is below the block size -1 ( $= NxM - 1$ ) The comparator 17 which outputs a high-level select signal (that is, when the result of an operation of an adder 13 is more than a block size ( $= NxM$ )), otherwise, outputs the select signal of a low level, When the select signal from a comparator 17 is high-level, the result of an operation of an adder 13 is made to input into the data terminal (D) of the F/F group 11. the selector 19 which makes the result of an operation of a subtractor 15 input into the data terminal (D) of the F/F group 11 when the select signal from a comparator 17 is a low level -- since -- it is constituted.

[0043] In addition, the F/F group 11 operates synchronizing with the standup of a clock, and sometimes, the reset signal inputted into the reset terminal (RESET) of self from reset-signal input terminal T four

memorizes the data value which is a low level and which is inputted into the data terminal (D) of self through an input bus from a selector 19 to the standup timing of a clock (latch), and usually outputs it to it from an output terminal (Q) to the address output terminal T5. Moreover, irrespective of the output of a selector 19, if a self output value becomes a block size -1 ( $=N \times M - 1$ ), the F/F group 11 consists of standup timing of the following clock so that it may return to 0 the output value of whose is initial value.

[0044] Thus, in the constituted address counter 3, if a high-level reset signal is inputted from reset-signal input terminal T four, the F/F group 11 will be the counted value which is reset synchronizing with the clock from the clock input terminal T1, consequently is memorized by the F/F group 11, and, as for the address outputted to memory, all bits will serve as the initial value 0 of 0 from the address output terminal T5 (refer to drawing 4 ).

[0045] And if the reset signal from reset-signal input terminal T four is set to a low level and reset is canceled, count-up actuation of the address to memory will be performed focusing on the F/F group 11 from the next clock after the reset discharge. As count-up actuation of this address counter 3, the step size inputted from the current output value and the current step size computing element 5 of the F/F group 11 is first added by the adder 13, and the size comparison of the result of an operation of that adder 13 and the value of a block size -1 ( $=N \times M - 1$ ) is carried out by the comparator 17.

[0046] and when the result of an operation of an adder 13 is below the block size -1 ( $=N \times M - 1$ ) By the selector 19 which operates according to the select signal from a comparator 17 The result of an operation of an adder 13 is inputted into the data terminal (D) of the F/F group 11 as it is. Consequently, the F/F group 11 While memorizing the result of an operation of an adder 13 as counted value of the address counter 3 concerned to the standup timing of the following clock, the memorized counted value will be outputted to the address output terminal T5 as the address to memory from a self output terminal (Q).

[0047] moreover, conversely, when the result of an operation of an adder 13 is more than a block size ( $=N \times M$ ) By the above-mentioned selector 19, the value which is the result of an operation of a subtractor 15, and subtracted the block size -1 ( $=N \times M - 1$ ) from the result of an operation of an adder 13 It is inputted into the data terminal (D) of the F/F group 11. Consequently, the F/F group 11 While memorizing the result of an operation of a subtractor 15 as counted value of the address counter 3 concerned to the standup timing of the following clock, the memorized counted value will be outputted to the address output terminal T5 as the address to memory from a self output terminal (Q).

[0048] Therefore, although count-up actuation will be performed from initial value 0 with the step size which synchronizes with a clock and is inputted from the step size computing element 5 according to an operation of the F/F group 11 and an adder 13 and the counted value will be outputted as the address to memory in an address counter 3 When the counted value in the following clock timing becomes more than a block size ( $=N \times M$ ) especially The value which took the modulo of a block size -1 ( $=N \times M - 1$ ) about the value more than the block size turns into counted value in the following clock timing according to an operation of a subtractor 15, a comparator 17, and a selector 19. And when the counted value in further this clock timing becomes a block size -1 ( $=N \times M - 1$ ), the counted value in the following clock timing will return to initial value 0 according to the operation of the F/F group 11 mentioned above.

[0049] As shown in drawing 3 , on the other hand, the step size computing element 5 An address counter 3 memorizes the step size used for the above-mentioned count-up actuation synchronizing with the clock from the clock input terminal T1. It is an address counter 3 (in detail) about the memorized step size. The flip-flop with [ 1st bit ] a clock synchronization preset feature outputted to the adder 13 of an address counter 3, The flip-flop group 21 (henceforth the F/F group 21) which except [ its ] becomes from a flip-flop with a clock synchronization reset function, The operation value produced from the F/F group 21 in the process in which the step size which should be outputted to an address counter 3 is calculated It has the flip-flop group 23 (henceforth the F/F group 23) which consists of a number corresponding to input bus width of face of flip-flops with a clock synchronization reset function memorized synchronizing with the clock from the clock input terminal T1.

[0050] In addition, the F/F groups 21 and 23 operate synchronizing with the standup of a clock, and sometimes, the signal inputted into self reset terminal (RESET) or presetting terminal (SET) memorizes the data value which is a low level and which is inputted into the data terminal (D) of self through an input bus to the standup timing of a clock (latch), and usually outputs them to it from an output terminal (Q). Moreover, the adder 25 with which the step size computing element 5 adds the output value (namely, step size which is carrying out the current output from the F/F group 21 to the address counter 3) of the F/F group 21, and the output value of the F/F group 23, The subtractor 27 which subtracts the block size -1 ( $=N \times M - 1$ ) inputted from the block-size input terminal T2 from the result of an operation of the adder 25, The size comparison of the result of an operation of an adder 25 and the block size -1 from the block-size input terminal T2 is carried out. When the result of an operation of an adder 25 is below the block size -1 ( $=N \times M - 1$ ) The comparator 29 which outputs a high-level select signal (that is, when the result of an operation of an adder 25 is more than a block size ( $=N \times M$ )), otherwise, outputs the select signal of a low level, When the select signal from a comparator 29 is high-level, the result of an operation of an adder 25 is chosen and outputted. The selector 31 which chooses and outputs the result of an operation of a subtractor 27 when the select signal from a comparator 29 is a low level, Data showing the number of columns inputted from the counted value (namely, address currently outputted to memory from the F/F group 11 of an address counter 3) of an address counter 3, and number input terminal T3 of columns (only below) A size comparison is carried out. the number of columns -- saying, when the counted value of an address counter 3 is smaller than the number of columns ( $=M$ ) The comparator 33 which outputs a high-level select signal (that is, when the counted value of an address counter 3 is more than the number of columns ( $=M$ )), otherwise, outputs the select signal of a low level, When the select signal from a comparator 33 is high-level, the output of a selector 31 is made to input into the data terminal (D) of the F/F group 23. When the select signal from a comparator 33 is a low level, it has the selector 35 which makes the output of the F/F group 23 input into the data terminal (D) of this F/F group 23.

[0051] And the step size computing element 5 compares the counted value of an address counter 3 with the block size -1 from the block-size input terminal T2 further. When the counted value of an address counter 3 is equal to a block size -1 ( $=N \times M - 1$ ) The comparator 37 which outputs a high-level select signal (that is, when the counted value of an address counter 3 is not equal to a block size -1 ( $=N \times M - 1$ )), otherwise, outputs the select signal of a low level, When the select signal from a comparator 37 is high-level, the output of the F/F group 23 is made to input into the data terminal (D) of the F/F group 21. The selector 39 which makes the output of the F/F group 21 input into the data terminal (D) of this F/F group 21 when the select signal from a comparator 37 is a low level, It has OR circuit 41 which makes the OR signal of the reset signal from reset-signal input terminal T four, and the select signal from a comparator 37 input into the reset terminal (RESET) of the F/F group 23.

[0052] Next, actuation of the step size computing element 5 constituted as mentioned above is explained. First, if a high-level reset signal is inputted from reset-signal input terminal T four, by the F/F group 23, the signal inputted into the reset terminal (RESET) of each of that flip-flop will become high-level through OR circuit 41, and will become high-level [ the signal inputted into the presetting terminal (SET) of the bit / 1st / flip-flop, and the reset terminal (RESET) of the flip-flop of the other bit, respectively ] in the F/F group 21.

[0053] For this reason, if a high-level reset signal is inputted from reset-signal input terminal T four, as for the output value of the F/F group 23, all bits will be set to 0 synchronizing with the clock from the clock input terminal T1. Moreover, the step size which the 1st bit is 1, and the other bit is set to 0 by the output value of the F/F group 21, consequently is outputted to an address counter 3 is set to 1 as initial value (refer to [drawing 4](#) ).

[0054] Then, if the reset signal from reset-signal input terminal T four is set to a low level and reset is canceled, the F/F group 23 will latch and output the output of the selector 35 which operates according to the select signal from a comparator 33 synchronizing with a clock.

[0055] A selector 35 makes the output of a selector 31 input into the data terminal (D) of the F/F group 23 here (namely, when for the address which is the counted value of an address counter 3 and is

outputted from the address output terminal T5 to be smaller than the number of columns ( $=M$ )), when the select signal from a comparator 33 is high-level.

[0056] And a selector 31 follows a select signal from a comparator 29. The result of an operation to which the output value of the F/F group 21 and the output value of the F/F group 23 were added by the adder 25 In being below the block size -1 ( $=N \times M - 1$ ) from the block-size input terminal T2 Output the result of an operation of the adder 25 to a selector 35 as it is, and conversely, when the result of an operation of an adder 25 is more than the block count ( $=N \times M$ ) The result of an operation by which the block size -1 ( $=N \times M - 1$ ) was subtracted from the result of an operation of an adder 25 with the subtractor 27 is outputted to a selector 35.

[0057] Moreover, a selector 35 makes the output of the F/F group 23 input into the data terminal (D) of the F/F group 23 (namely, when it to be the present counted value of an address counter 3 and for the address currently outputted from the address output terminal T5 to be more than the number of columns ( $=M$ )), when the select signal from a comparator 33 is a low level.

[0058] therefore, when the counted value of an address counter 3 is smaller than the number of columns ( $=M$ ), the F/F group 23 The value which took the modulo of a block size -1 ( $=N \times M - 1$ ) about the value adding a self current output value and the output value of the F/F group 23 It will hold without latching to the following clock timing, and updating a self output value, when the counted value of an address counter 3 is more than the number of columns ( $=M$ ).

[0059] The F/F group 23 consequently, by operating in collaboration with an adder 25, a subtractor 27, comparators 29 and 33, and selectors 31 and 35 While only column several M batches carry out accumulation of the step size currently outputted from the F/F group 21 during the period for [ until the counted value of an address counter 3 serves as a block size -1 ( $=N \times M - 1$ ) from initial value 0 ] 1 block The value which took the modulo of a block size -1 ( $=N \times M - 1$ ) about the accumulation value will be memorized as a new step size at the time of the interleave processing to the following block. And the value which took the modulo of a block size -1 ( $=N \times M - 1$ ) by this actuation about the value which multiplied the step size which is carrying out the current output to the address counter 3 by the number of columns ( $=M$ ) is set up as a new step size at the time of the interleave processing to the following block.

[0060] Moreover, if the counted value of an address counter 3 becomes a block size -1 ( $=N \times M - 1$ ), a comparator 37 will judge that it is the last entry-of-data timing of a block, and will output a high-level select signal. And the high-level select signal from the comparator 37 is inputted into the reset terminal (RESET) of the F/F group 23 through OR circuit 41. Therefore, the F/F group 23 will be reset to the following clock timing (namely, timing which the counted value of an address counter 3 is the timing which returns to initial value 0, and inputs the data of the beginning of the following block), and the output value will return to 0. That is, the high-level select signal outputted from a comparator 37 is an end-of-block signal meaning 1-block termination.

[0061] On the other hand, if the reset signal from reset-signal input terminal T four is set to a low level from high level and reset is canceled in the step size computing element 5 concerned, the F/F group 21 will latch the output of the selector 39 which operates according to the select signal from a comparator 37 synchronizing with a clock, and will output it as a step size.

[0062] When the select signal from a comparator 37 of a selector 39 is a low level here Namely, (when the counted value of an address counter 3 is not a block size -1 ( $=N \times M - 1$ )) The output of the F/F group 21 is made to input into the data terminal (D) of the F/F group 21. Moreover, when the select signal from a comparator 37 is high-level, the output of the F/F group 23 is made to input into the data terminal (D) of the F/F group 21 (namely, when for the counted value of an address counter 3 to be a block size -1 ( $=N \times M - 1$ )).

[0063] Therefore, the F/F group 21 is the following clock timing (namely, timing from which the counted value of an address counter 3 returns to initial value 0), when the counted value of an address counter 3 becomes a block size -1 ( $=N \times M - 1$ ). The new step size to the following block memorized by the F/F group 23 just before that is latched. The latched step size will be outputted to an address counter 3 during the period for [ until the counted value of an address counter 3 returns from a block size -1 ( $=$

$N \times M - 1$ ) to initial value 0 next ] 1 block.

[0064] That is, the F/F group 21 will output the memorized new step size to an address counter 3, while memorizing the new step size latched to the F/F group 23 to the following clock timing, if it is detected that the counted value of an address counter 3 became a block size -1 ( $= N \times M - 1$ ) with the comparator 37 by operating in collaboration with a selector 39. And the step size with which the counted value of an address counter 3 is outputted to that address counter 3 by this actuation synchronizing with the timing which returned to initial value 0 is changed into a new step size.

[0065] Next, drawing 4 is a timing diagram which mentions as an example the case where the interleave address generation machine 1 mentioned above is operated in interleave processing with a block size with a line count (low number)  $N = 4$  and  $M = 3$  trains (the number of columns), and expresses it. In addition, when the interleave address generation machine 1 of this operation gestalt is used, synchronizing with the clock to the clock input terminal T1, the sequential input of the data is carried out to memory.

[0066] The period which inputs the data (D 1-1 - D 1-12) of the 1st block in the case of this example as shown in drawing 4 In (namely, the period for 12 periods of the clock which is equivalent to 1 block of data from from just before a reset signal changes from high level to a low level) From an address counter 3, the address will be outputted in order of 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11. This is because the initial value of the step size outputted from the F/F group 21 of the step size computing element 5 is 1.

[0067] According to moreover, an operation of the circuit part which consists of the F/F group 23 of the step size computing element 5, an adder 25, a subtractor 27, comparators 29 and 33, and selectors 31 and 35 in this period While accumulation of the step size ( $= 1$ ) by which the current output is carried out from the F/F group 21 is carried out at each \*\*\*\* of 0, 1, and 2 with the address smaller than the number M of columns ( $= 3$ ) from an address counter 3 The value ( $= 3$ ) which took the modulo of a block size -1 ( $= 11$ ) about the accumulation value is memorized by the F/F group 23 as a new step size to the following block. In addition, since it does not become more than a block size ( $= 12$ ) in this case even if it carries out accumulation of the step size 3 times, the value memorized by the F/F group 23 changes with  $0 \rightarrow 1 \rightarrow 2 \rightarrow 3$ .

[0068] When the address outputted from an address counter 3 returns to 0 from 11, and to the timing While the new step size ( $= 3$ ) memorized by the F/F group 23 is latched to the F/F group 21 The new step size ( $= 3$ ) with which the output value of the F/F group 23 was latched to 0 by return and the F/F group 21 will be outputted to an address counter 3 as a step size in the period which inputs the data (D 2-1 - D 2-12) of the 2nd block.

[0069] For this reason, in the period which inputs the data (D 2-1 - D 2-12) of the 2nd block, the address will be outputted from an address counter 3 in order of 0, 3, 6, 9, 1, 4, 7, 10, 2, 5, 8, and 11. That in addition, the address outputted is changing to the degree of 9 in this period 1 Since the value ( $= 12$ ) which added 3 which is a current step size to 9 becomes more than a block size ( $= 12$ ), in this case 1 which is the result of an operation of a subtractor 15, and is the value which took the modulo of a block size -1 ( $= 11$ ) about 12 is because it is latched to the F/F group 11 as following counted value. And this is the same also about the case where the address outputted changes to the degree of 10 2.

[0070] According to moreover, an operation of the circuit part which consists of the F/F group 23 of the step size computing element 5, an adder 25, a subtractor 27, comparators 29 and 33, and selectors 31 and 35 in this period While accumulation of the step size ( $= 3$ ) by which the current output is carried out from the F/F group 21 is carried out at each \*\*\*\* of 0, 1, and 2 with the address smaller than the number M of columns ( $= 3$ ) from an address counter 3 The value ( $= 9$ ) which took the modulo of a block size -1 ( $= 11$ ) about the accumulation value is memorized by the F/F group 23 as a new step size to the following block. In addition, since it does not become more than a block size ( $= 12$ ) in this case even if it carries out accumulation of the step size 3 times, the value memorized by the F/F group 23 changes with  $0 \rightarrow 3 \rightarrow 6 \rightarrow 9$ .

[0071] When the address outputted from an address counter 3 returns to 0 from 11, and to the timing While the new step size ( $= 9$ ) memorized by the F/F group 23 is latched to the F/F group 21 The new

step size (= 9) with which the output value of the F/F group 23 was latched to 0 by return and the F/F group 21 will be outputted to an address counter 3 as a step size in the period which inputs the data (D 3-1 - D 3-12) of the 3rd block.

[0072] For this reason, in the period which inputs the data (D 3-1 - D 3-12) of the 3rd block, the address will be outputted from an address counter 3 in order of 0, 9, 7, 5, 3, 1, 10, 8, 6, 4, 2, and 11. That in addition, the address outputted is changing to the degree of 9 in this period 7 Since the value (= 18) which added 9 which is a current step size to 9 becomes more than a block size (= 12), in this case 7 which is the result of an operation of a subtractor 15, and is the value which took the modulo of a block size -1 (= 11) about 18 is because it is latched to the F/F group 11 as following counted value. And this is the same also about the case where the address outputted changes to the degree of 7 5, and the case where it changes to the degree of 5 3.

[0073] According to moreover, an operation of the circuit part which consists of the F/F group 23 of the step size computing element 5, an adder 25, a subtractor 27, comparators 29 and 33, and selectors 31 and 35 in this period While accumulation of the step size (= 9) by which the current output is carried out from the F/F group 21 is carried out at each \*\*\*\* of 0, 1, and 2 with the address smaller than the number M of columns (= 3) from an address counter 3 The value (= 5) which took the modulo of a block size -1 (= 11) about the accumulation value is memorized by the F/F group 23 as a new step size to the following block. In addition, the value memorized by the F/F group 23 in this case changes with 0->9->7->5.

[0074] Although not shown in drawing 4, when the address outputted from an address counter 3 returns to 0 from 11 after that, and to the timing While the new step size (= 5) memorized by the F/F group 23 is latched to the F/F group 21 The new step size (= 5) with which the output value of the F/F group 23 was latched to 0 by return and the F/F group 21 will be outputted to an address counter 3 as a step size in the period which inputs the data of the 4th block. For this reason, in the period which inputs the data of the 4th block, the address will be outputted from an address counter 3 in order of 0, 5, 10, 4, 9, 3, 8, 2, 7, 1, 6, and 11.

[0075] as mentioned above, with the interleave address generation vessel 1 of a \*\*\*\* 1 operation gestalt, whenever the address outputted returns from a block size -1 (=  $N \times M - 1$ ) to initial value 0, it will come out, and there will be a step size of the address outputted from an address counter 3 synchronizing with a clock, and it will be changed by the step size computing element 5 for every 1 block of input data.

[0076] Therefore, according to this interleave address generation machine 1, it sets at the period which inputs the data of the 1st block. In the period which inputs the data of each block of input data of sequential writing and the 2nd henceforth into each address of the memory outputted from an address counter 3 While reading data from each address of the memory outputted from an address counter 3 By overwriting the present input data to the read address, as mentioned already using drawing 1, addressing of the read-out of the data from memory will be carried out with a different step size from the time of writing in the data. For example, in the case of the example shown in drawing 4, supposing it attaches to order D1, D2, D3, D4, D5, D6, D7, D8, D9, and an index called D10, D11, and D12 from the 1st thing to the input data for 1 block The input data of each block by which a sequential input is carried out will be rearranged into the sequence of D1, D4, D7, D10 and D2, D5, D8, D11 and D3, D6, D9, and D12 by being read from memory, respectively.

[0077] For this reason, according to the interleave address generation machine 1 of a \*\*\*\* 1 operation gestalt, only by having 1 set of the interleave address generation machine 1 concerned and memory, the continuous interleave processing to the data of two or more blocks is attained, and the circuit (interleave circuit) for performing interleave processing can be miniaturized.

[0078] In addition, with the \*\*\*\* 1 operation gestalt, the address counter 3 is equivalent to the address count means, and actuation of the address counter 3 is equivalent to address count processing. Moreover, the step size computing element 5 is equivalent to the step size operation means, and actuation of the step size computing element 5 is equivalent to step size setting processing. And among each part which constitutes the step size computing element 5, the F/F group 23, an adder 25, a subtractor 27, comparators 29 and 33, selectors 31 and 35, and OR circuit 41 are equivalent to a step size setting means

according to claim 2, a comparator 37 is equivalent to a detection means according to claim 2, and the F/F group 21 and the selector 39 are equivalent to the step size output means according to claim 2.

[0079] By the way, although the value which multiplied the step size which is carrying out the current output to the address counter 3 by the number M of columns was calculated with the interleave address generation vessel 1 of the above-mentioned 1st operation gestalt when only column several M batches carried out accumulation of the current step size, it may be made to carry out the direct multiplication of a current step size and the number M of columns.

[0080] then -- next, a current step size -- several columns -- the value which multiplied by M -- a current step size and several columns -- the interleave address generation machine of the 2nd operation gestalt for which it asked by carrying out the multiplication of M with a multiplier is explained concretely. First, drawing 5 is a circuit diagram showing the interleave address generation machine 43 of a \*\*\*\* 2 operation gestalt. In addition, in drawing 5, about the same component as the interleave address generation machine 1 of the 1st operation gestalt mentioned above, since the same sign is attached, detailed explanation is omitted.

[0081] As shown in drawing 5, as compared with the interleave address generation machine 1 of the 1st operation gestalt, only the configurations of the step size computing element 45 differ, and the address counter 3 of the interleave address generation machine 43 of a \*\*\*\* 2 operation gestalt is completely the same. And the step size computing element 45 of a \*\*\*\* 2 operation gestalt It compares with the step size computing element 5 of the 1st operation gestalt. Instead of an adder 25, a subtractor 27, comparators 29 and 33, selectors 31 and 35, and OR circuit 41 The multiplier 47 which carries out the multiplication of the output value (namely, current step size) of the F/F group 21, and the number of columns from number input terminal T3 of columns (=M), When the counted value (namely, address currently outputted to memory from the F/F group 11 of an address counter 3) of an address counter 3 is 0 The comparator 49 which outputs a high-level select signal, and outputs the select signal of a low level when the counted value of an address counter 3 is not 0, The selector 51 which chooses and outputs the result of an operation of a multiplier 47 when the select signal from a comparator 49 is high-level, and chooses and outputs the output of the F/F group 23 when the select signal from a comparator 49 is a low level, The subtractor 53 which subtracts the block size -1 (=NxM -1) inputted from the block-size input terminal T2 from the output of the selector 51, The size comparison of the output of a selector 51 and the block size -1 from the block-size input terminal T2 is carried out. When the output of a selector 51 is below the block size -1 (=NxM -1) The comparator 55 which outputs a high-level select signal (that is, when the output of a selector 51 is more than a block size (=NxM)), otherwise, outputs the select signal of a low level, When the select signal from a comparator 55 is high-level, the output of a selector 51 is made to input into the data terminal (D) of the F/F group 23. When the select signal from a comparator 55 is a low level, it has the selector 57 which makes the result of an operation of a subtractor 53 input into the data terminal (D) of the F/F group 23.

[0082] And in this step size computing element 45, the direct input of the reset signal from reset-signal input terminal T four is carried out to the reset terminal (RESET) of the F/F group 23. Thus, in the constituted step size computing element 45, if a high-level reset signal is inputted from reset-signal input terminal T four, by the F/F group 23, the signal inputted into the reset terminal (RESET) of each of that flip-flop will become high-level, and the signal inputted into the presetting terminal (SET) of the bit [ 1st ] flip-flop and the reset terminal (RESET) of the flip-flop of the other bit, respectively will become high-level by the F/F group 21.

[0083] For this reason, like the step size computing element 5 of the 1st operation gestalt, if a high-level reset signal is inputted from reset-signal input terminal T four, as for the output value of the F/F group 23, all bits will be set to 0 synchronizing with the clock from the clock input terminal T1. Moreover, the step size which the 1st bit is 1, and the other bit is set to 0 by the output value of the F/F group 21, consequently is outputted to an address counter 3 is set to 1 as initial value (refer to drawing 6).

[0084] And if the reset signal from reset-signal input terminal T four is set to a low level and reset is canceled after that, the F/F group 23 will latch and output the output of a selector 57 synchronizing with a clock. It sets to the step size computing element 45 of a \*\*\*\* 2 operation gestalt here. When the

counted value of an address counter 3 is 0, from a selector 51 The multiplication result to which the multiplication of the output value and the number of columns ( $=M$ ) of the F/F group 21 was carried out by the multiplier 47 is outputted, and further, if the multiplication result of the multiplier 47 is below the block size -1 ( $=NxM -1$ ) The multiplication result is outputted to the data terminal (D) of the F/F group 23 from a selector 57 as it is, and with [ the result of an operation of a multiplier 47 ] the block count [ more than ] ( $=NxM$ ), conversely The result of an operation by which the block size -1 ( $=NxM -1$ ) was subtracted from the multiplication result of a multiplier 47 with the subtractor 53 is outputted to the data terminal (D) of the F/F group 23 from a selector 57.

[0085] moreover, when the counted value of an address counter 3 is not 0 The direction of the output of the F/F group 23 is chosen and outputted from a selector 51, and further, if the output value of the F/F group 23 is below the block size -1 ( $=NxM -1$ ) The output of the F/F group 23 is outputted to the data terminal (D) of the F/F group 23 from a selector 57 as it is, and with [ the output value of the F/F group 23 ] the block count [ more than ] ( $=NxM$ ), conversely The result of an operation by which the block size -1 ( $=NxM -1$ ) was subtracted from the output value of the F/F group 23 with the subtractor 53 is outputted to the data terminal (D) of the F/F group 23 from a selector 57.

[0086] For this reason, the F/F group 23 will memorize the value which took the modulo of a block size -1 ( $=NxM -1$ ) about the multiplication value which carried out the multiplication of the step size currently outputted from the F/F group 21, and the number M of columns as a new step size at the time of the interleave processing to the following block by operating in collaboration with a multiplier 47, a subtractor 53, comparators 49 and 55, and selectors 51 and 57. And the value which took the modulo of a block size -1 ( $=NxM -1$ ) by this actuation about the value which multiplied the step size which is carrying out the current output to the address counter 3 by the number of columns ( $=M$ ) is set up as a new step size at the time of the interleave processing to the following block.

[0087] On the other hand, if the reset signal from reset-signal input terminal T four is set to a low level from high level and reset is canceled like the step size computing element 5 of the 1st operation gestalt also in the step size computing element 45 concerned, the F/F group 21 will latch the output of the selector 39 which operates according to the select signal from a comparator 37 synchronizing with a clock, and will output it as a step size. And when the select signal from a comparator 37 of a selector 39 is a low level Namely, (when the counted value of an address counter 3 is not a block size -1 ( $=NxM -1$ )) The output of the F/F group 21 is made to input into the data terminal (D) of the F/F group 21. Moreover, when the select signal from a comparator 37 is high-level, the output of the F/F group 23 is made to input into the data terminal (D) of the F/F group 21 (namely, when for the counted value of an address counter 3 to be a block size -1 ( $=NxM -1$ )).

[0088] Also in the step size computing element 45 of a \*\*\*\* 2 operation gestalt therefore, the F/F group 21 When the counted value of an address counter 3 becomes a block size -1 ( $=NxM -1$ ), to the following clock timing (namely, timing from which the counted value of an address counter 3 returns to initial value 0) The new step size to the following block memorized by the F/F group 23 is latched. The latched step size will be outputted to an address counter 3 during the period for [ until the counted value of an address counter 3 returns from a block size -1 ( $=NxM -1$ ) to initial value 0 next ] 1 block.

[0089] Here, drawing 6 is a timing diagram which mentions as an example the case where operate the interleave address generation machine 43 of a \*\*\*\* 2 operation gestalt, and it operates interleave processing with a block size with a line count (low number)  $N=4$  and  $M=3$  trains (the number of columns), and expresses it. As shown in drawing 6, and with the interleave address generation vessel 43 of a \*\*\*\* 2 operation gestalt In initiation of a period to the 2nd clock timing to input [ of the F/F group 23 ] the data (D 1-1 - D 1-12) of the 1st block In initiation of a period to the 2nd clock timing which changes to 0-3 and inputs the data (D 2-1 - D 2-12) of the 2nd block In initiation of a period to the 2nd, and each 3rd clock timing which changes to 9 from 3 and inputs the data (D 3-1 - D 3-12) of the 3rd block further Only the point which carries out sequential change with 9->16->5 differs from the interleave address generation machine 1 of the 1st operation gestalt.

[0090] And also with such an interleave address generation vessel 43 of a \*\*\*\* 2 operation gestalt, the address will be outputted in the completely same sequence as the interleave address generation machine

1 of the 1st operation gestalt, it only has 1 set of of the interleave address generation machine 43 concerned and memory, and the continuous interleave processing to the data of two or more blocks is attained from an address counter 3.

[0091] In addition, with the \*\*\*\* 2 operation gestalt, the address counter 3 is equivalent to the address count means, and actuation of the address counter 3 is equivalent to address count processing. Moreover, the step size computing element 45 is equivalent to the step size operation means, and actuation of the step size computing element 45 is equivalent to step size setting processing. And among each part which constitutes the step size computing element 45, the F/F group 23, a multiplier 47, a subtractor 53, comparators 49 and 55, and selectors 51 and 57 are equivalent to a step size setting means according to claim 3, a comparator 37 is equivalent to a detection means according to claim 3, and the F/F group 21 and the selector 39 are equivalent to the step size output means according to claim 3.

[0092] As mentioned above, although 1 operation gestalt of this invention was explained, it cannot be overemphasized that this invention is not limited to the operation gestalt mentioned above, and various gestalten can be taken. For example, although the initial value of the step size outputted to an address counter 3 from the step size computing elements 5 and 45 was 1 with each operation gestalt mentioned above, the initial value of a step size should just be one or more integers.

[0093] Moreover, what is necessary is to add the value of the start address of memory to the address outputted from an address counter 3, and just to make it supply the address after the addition to it at the address input terminal of memory, when the number of the start addresses of the memory used for interleave processing is not zero.

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[Translation done.]

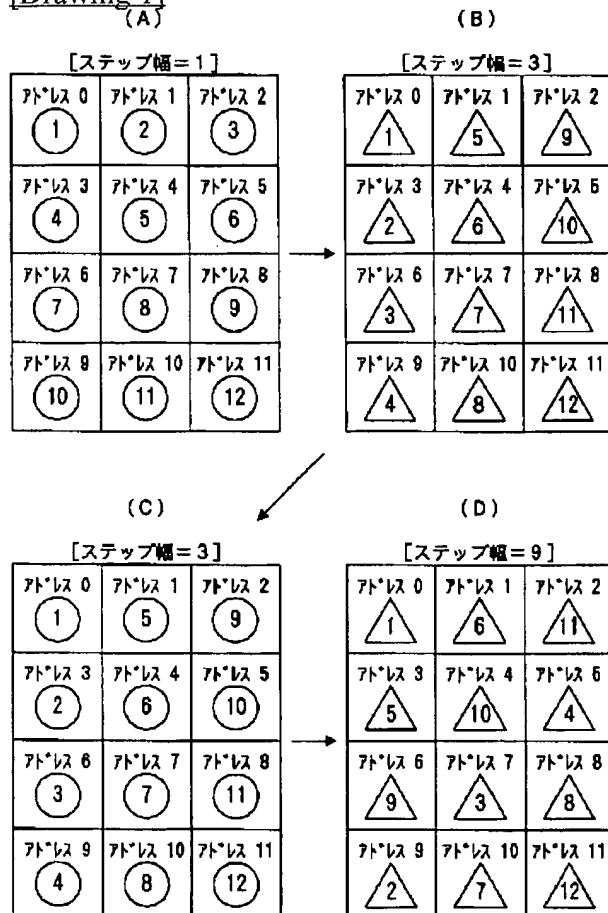
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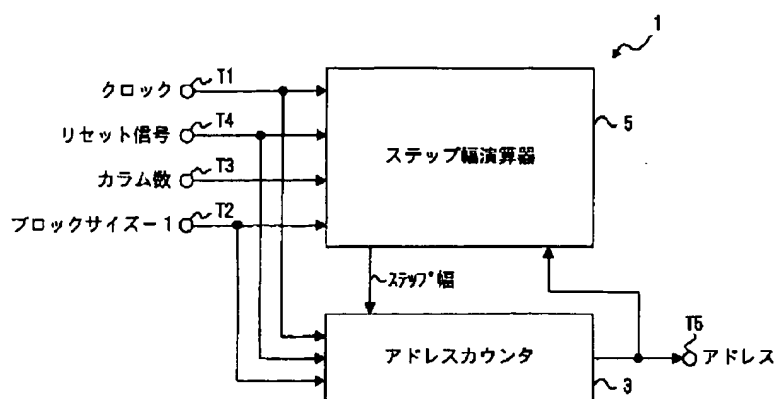
1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

## DRAWINGS

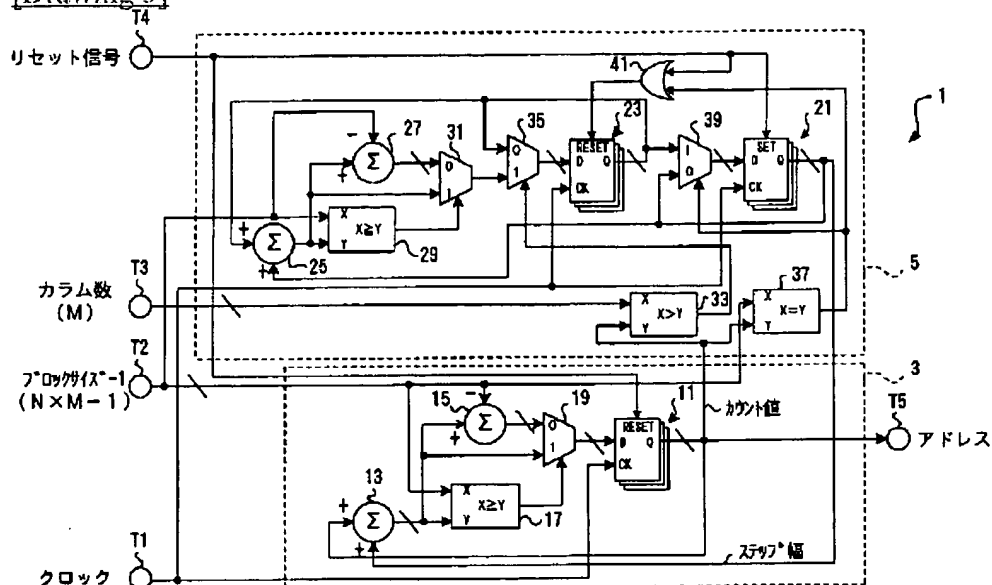
[Drawing 1]



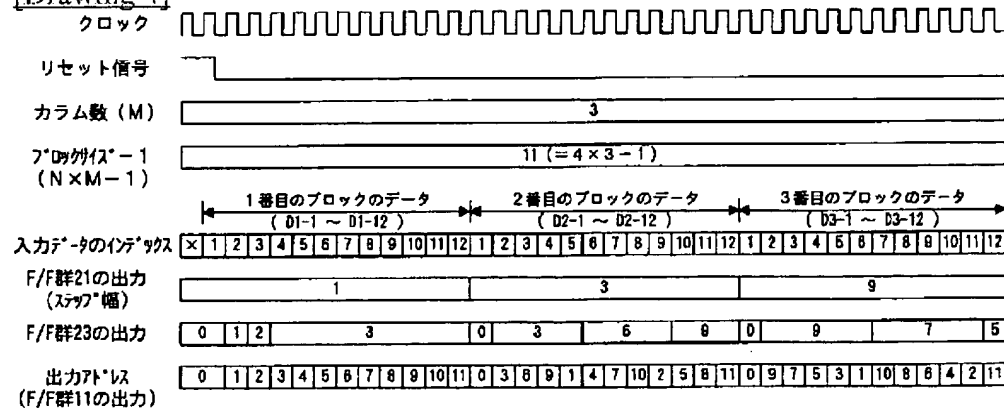
[Drawing 2]



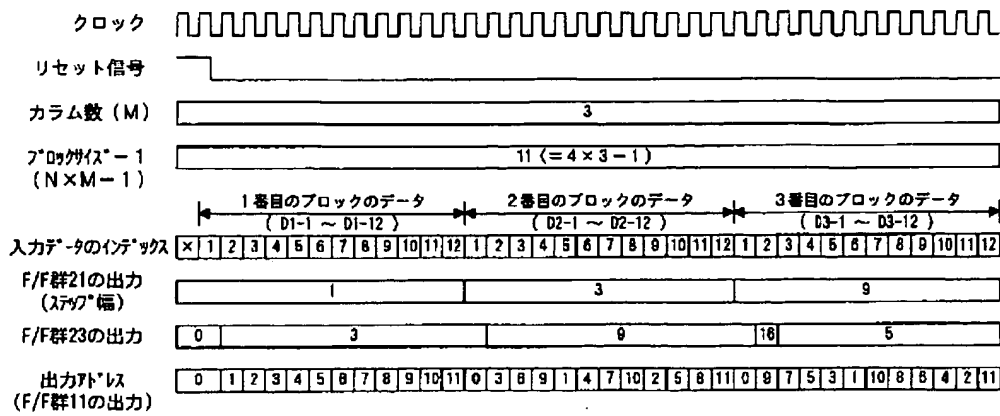
[Drawing 3]



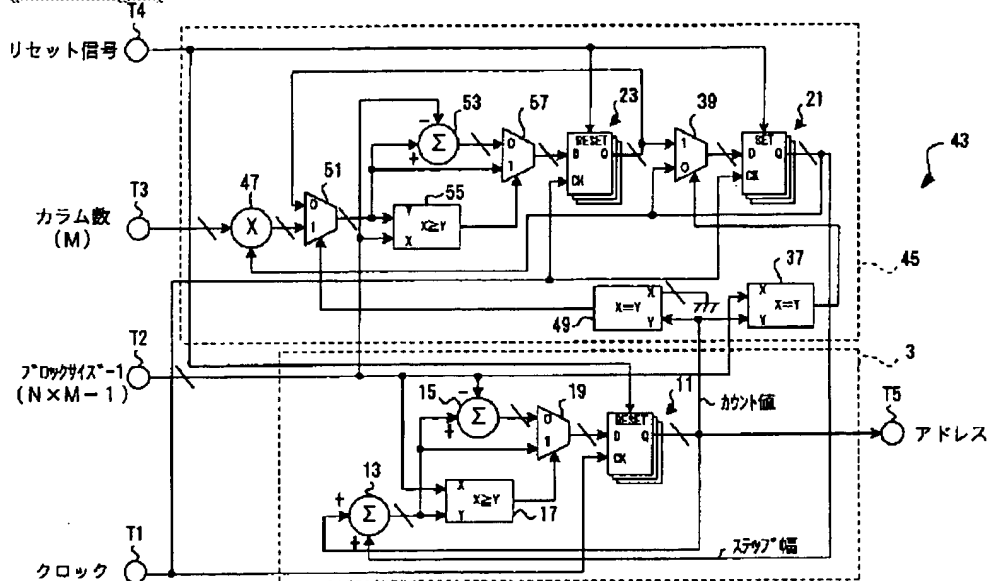
[Drawing 4]



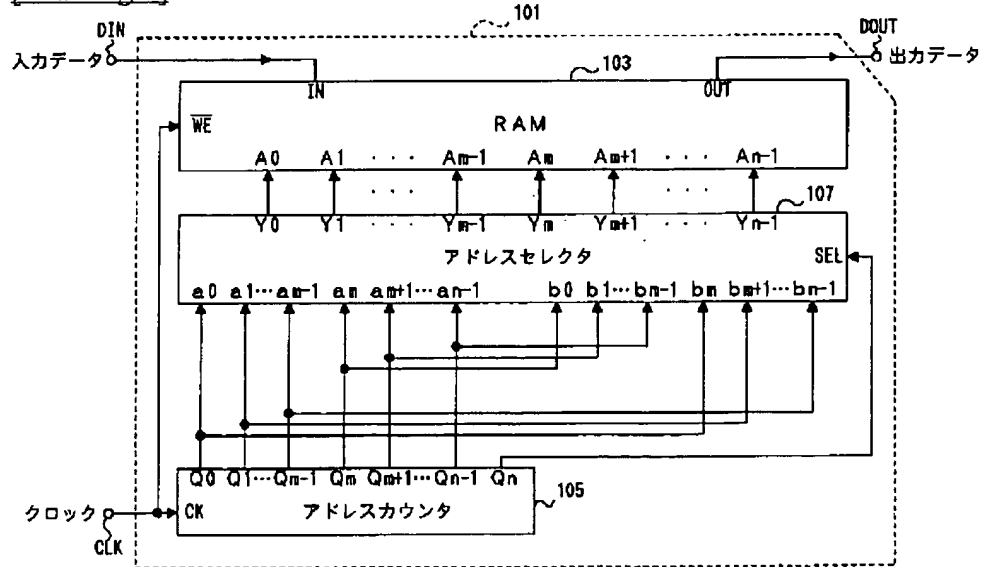
[Drawing 6]



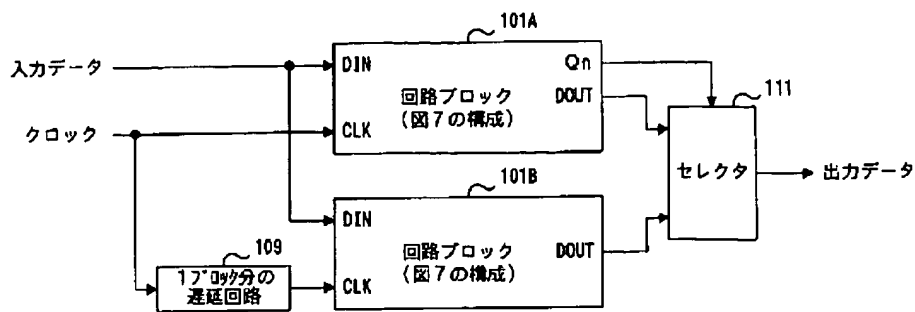
[Drawing 5]



[Drawing 7]



[Drawing 9]



[Drawing 8]

(A)

(B)

行(ロー)方向 → 書き込み

アドレス 0 1	アドレス 1 2	アドレス 2 3	アドレス 3 4
アドレス 4 5	アドレス 5 6	アドレス 6 7	アドレス 7 8
アドレス 8 9	アドレス 9 10	アドレス 10 11	アドレス 11 12
アドレス 12 13	アドレス 13 14	アドレス 14 15	アドレス 15 16

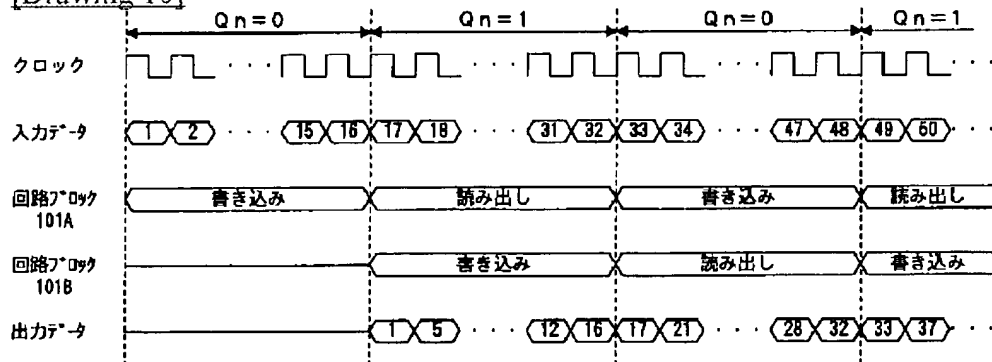
(○内の番号は、データを書き込む順序)

列(コラム)方向 ↓ 読み出し

アドレス 0 1	アドレス 1 5	アドレス 2 9	アドレス 3 13
アドレス 4 2	アドレス 5 6	アドレス 6 10	アドレス 7 14
アドレス 8 3	アドレス 9 7	アドレス 10 11	アドレス 11 15
アドレス 12 4	アドレス 13 8	アドレス 14 12	アドレス 15 16

(△内の番号は、データを読み出す順序)

[Drawing 10]



[Translation done.]

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3. In the drawings, any words are not translated.

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## EFFECT OF THE INVENTION

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[The means for solving a technical problem and an effect of the invention] The interleave address generation approach of this invention made in order to attain the above-mentioned purpose While carrying out the sequential input of the data according to claim 4 which make 1 block a  $N \times M$  individual (however,  $M \geq N$  and  $N \geq 2$  or more integers) like and writing in memory By reading in order of the address which writes in the data written in the memory and is different from the time It is used in order to perform interleave processing which outputs the inputted data in different sequence from the sequence at the time of an input, and read-out in said memory and the address for writing are generated.

[0018] And the interleave address generation approach of this invention While performing count-up from initial value 0 with the set-up step size and carrying out the sequential output of the counted value as read-out in said memory, and the address for writing When the following counted value becomes beyond the above ( $N \times M$ ) When it considers as the following counted value and further this counted value becomes ( $N \times M - 1$ ), the value which took the modulo of ( $N \times M - 1$ ) about the value Address count processing in which the following counted value was returned to initial value 0, It consists of step size setting processing in which said step size used by this address count processing is set up. In step size setting processing The value which took the modulo of ( $N \times M - 1$ ) about the value which multiplied the step size which is carrying out a current setup by said  $M$  Ask as a new step size at the time of the interleave processing to the following block, and it synchronizes with the timing from which the counted value by said address count processing returned to initial value 0. It is characterized by updating the step size used by said address count processing to said new step size for which it asked.

[0019] Moreover, such an interleave address generation approach of this invention can be enforced with an interleave address generation vessel according to claim 1. Namely, an interleave address generation circuit according to claim 1 While carrying out the sequential input of the data which make 1 block a  $N \times M$  individual (however,  $M \geq N$  and  $N \geq 2$  or more integers) and writing in memory By reading in order of the address which writes in the data written in the memory and is different from the time It is used in order to perform interleave processing which outputs the inputted data in different sequence from the sequence at the time of an input, and read-out in said memory and the address for writing are generated, and it has the address count means and the step size operation means.

[0020] And count-up actuation is performed from initial value 0 with the step size which an address count means synchronizes with a clock, and is inputted from the exterior. While outputting the counted value as read-out in said memory, and the address for writing, when the counted value in the following clock timing becomes beyond the above ( $N \times M$ ) When the value which took the modulo of ( $N \times M - 1$ ) about the value is made into the counted value in the following clock timing and further this counted value becomes ( $N \times M - 1$ ), it is constituted so that the counted value in the following clock timing may be returned to initial value 0.

[0021] And further, although a step size operation means calculates the step size used for count-up actuation and an address count means outputs it to said address count means The value which took the modulo of ( $N \times M - 1$ ) especially about the value which multiplied the step size which is carrying out the current output by said  $M$  It sets up as a new step size at the time of the interleave processing to the

following block, and the step size outputted to said address count means is changed into said set-up new step size synchronizing with the timing from which the counted value of said address count means returned to initial value 0.

[0022] In addition, the step size means the value of the increment in every time at the time of counting up the counted value used as the address to memory. Moreover, the value which took the modulo of  $(NxM - 1)$  about a certain value  $Z$  means too much value at the time of breaking a certain value  $Z$  by  $(NxM - 1)$ .

[0023] in the interleave address generation approach and interleave address generation machine of such this invention, it will come out and there will be a step size of the address outputted by address count processing or the address count means, whenever the address outputted returns from  $(NxM - 1)$  to initial value 0, and it will be changed for every 1 block of input data.

[0024] Therefore, according to the interleave address generation approach and interleave address generation machine of this invention, it sets at the period which inputs the data of the 1st block (namely, beginning). Input data to each address of the memory outputted by address count processing or the address count means Sequential writing, In the period which inputs the data of each block of the 2nd henceforth While reading data from each address of the memory outputted by address count processing or the address count means By overwriting current input data to the read address, addressing of the read-out of the data from memory will be carried out with a different step size from the time of writing in the data. For this reason, the continuous interleave processing to the data of two or more blocks is attained only by having memory and an interleave address generation machine 1 set.

[0025] For example, while setting initial value of a step size to 1, the case where interleave processing is performed with a block size with a line count (low number)  $N=4$  and  $M=3$  trains (the number of columns) is explained concretely (namely, when performing interleave processing in four line x3 train which made 4x3 data 1 block).

[0026] In this case, as shown in the 5th step and the bottom from on drawing 4, in the period which inputs the data (D 1-1 - D 1-12) of the 1st block, the address will be outputted from address count processing or an address count means in order of 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11.

[0027] And it sets at the period which inputs the data (D 2-1 - D 2-12) of the 2nd block, and the step size set up or outputted by step size setting processing or the step size operation means serves as a value (= 3) which took the modulo of 11 ( $=NxM - 1$ ) about the value (= 3) which multiplied the step size (= 1) in the input period of the 1st block by  $M (= 3)$ . Therefore, from address count processing or an address count means, the address will be outputted in order of 0, 3, 6, 9, 1, 4, 7, 10, 2, 5, 8, and 11. In addition, since the value (= 12) which added 3 which is a current step size to 9 becomes more than 12 ( $=NxM$ ) that is the number of data of 1 block, the address outputted is changing to the degree of 9 1 because 1 which is the value which took the modulo of 11 ( $=NxM - 1$ ) about 12 in this case becomes the following counted value. Moreover, since the value (= 13) to which that the address outputted is changing to the degree of 10 similarly 2 also added 3 which is a current step size to 10 becomes more than 12 ( $=NxM$ ), 2 which is the value which took the modulo of 11 ( $=NxM - 1$ ) about 13 in this case is because it becomes the following counted value.

[0028] And it sets further at the period which inputs the data (D 3-1 - D 3-12) of the 3rd block, and the step size set up or outputted by step size setting processing or the step size operation means serves as a value (= 9) which took the modulo of 11 ( $=NxM - 1$ ) about the value (= 9) which multiplied the step size (= 3) in the input period of the 2nd block by  $M (= 3)$ . Therefore, from address count processing or an address count means, the address will be outputted in order of 0, 9, 7, 5, 3, 1, 10, 8, 6, 4, 2, and 11. In addition, since the value (= 18) which added 9 which is a current step size to 9 becomes more than 12 ( $=NxM$ ) that is the number of data of 1 block, the address outputted is changing to the degree of 9 7 because 7 which is the value which took the modulo of 11 ( $=NxM - 1$ ) about 18 in this case becomes the following counted value. And this is the same also about the case where the address outputted changes to the degree of 7 5, and the case where it changes to the degree of 5 3.

[0029] Moreover, although not shown in drawing 4, it sets at the period which inputs the data of the 4th block, and the step size set up or outputted by step size setting processing or the step size operation

means serves as a value ( $= 5$ ) which took the modulo of  $11 (= NxM - 1)$  about the value ( $= 27$ ) which multiplied the step size ( $= 9$ ) in the input period of the 3rd block by  $M (= 3)$ . Therefore, from address count processing or an address count means, the address will be outputted in order of 0, 5, 10, 4, 9, 3, 8, 2, 7, 1, 6, and 11. In addition, since the value ( $= 15$ ) which added 5 which is a current step size to 10 becomes more than 12 ( $= NxM$ ) that is the number of data of 1 block, the address outputted is changing to the degree of 10 4 because 4 which is the value which took the modulo of  $11 (= NxM - 1)$  about 15 in this case becomes the following counted value. And this is the same also about the case where the address outputted changes to the degree of 9 3, and the case where it changes to the degree of 8 2.

[0030] Therefore, if the data of the 1st block are written in each address of the memory outputted by address count processing or the address count means one by one, each data of the 1st block will be written in the addresses from 0 to 11 of memory in order of the number shown in O of drawing 1 (A).

[0031] And while reading data from each address of the memory outputted by address count processing or the address count means in the period which inputs the data of the 2nd block If current input data is overwritten to the read address, each data of the 1st block already written in memory It is read from the addresses from 0 to 11 in order of the number shown in \*\* of drawing 1 (B). Moreover, each data of the 2nd block It will be written in the addresses from 0 to 11 of memory in order of the number shown in O of drawing 1 (C) (namely, the same sequence as the number shown in \*\* of drawing 1 (B)).

[0032] And further, in the period which inputs the data of the 3rd block, while reading data from each address of the memory outputted by address count processing or the address count means If current input data is overwritten to the read address, each data of the 2nd block already written in memory It is read from the addresses from 0 to 11 in order of the number shown in \*\* of drawing 1 (D). Moreover, each data of the 3rd block It will be written in the addresses from 0 to 11 of memory like the relation between drawing 1 (B) and drawing 1 (C) in order of the number shown in \*\* of drawing 1 (D).

[0033] For this reason, supposing it attaches to order D1, D2, D3, D4, D5, D6, D7, D8, D9, and an index called D10, D11, and D12 from the 1st thing to 12 input data for 1 block The input data of each block by which a sequential input is carried out so that the relation between drawing 1 (A) and drawing 1 (B) and the relation between drawing 1 (C) and drawing 1 (D) may also show By being read from memory, it will be rearranged into the sequence of D1, D4, D7, D10 and D2, D5, D8, D11 and D3, D6, D9, and D12, respectively.

[0034] That is, the interleave processing which continued only by one memory is attained by changing the step size of the address to memory for every 1 block of data with step size setting processing or a step size operation means. In addition, the initial value of a step size is not restricted to 1, and should just be one or more integers. Moreover, what is necessary is to add the address value of the above-mentioned head to the address outputted by address count processing or the address count means, and just to make it supply the address after the addition to the address input terminal of memory, when the number of the start addresses of the memory used for interleave processing is not zero.

[0035] In an interleave address generation machine according to claim 1 by the way, a step size operation means While only said M batch carries out accumulation of the step size according to claim 2 which is carrying out the current output like during the period for [ until the counted value of an address count means serves as  $(NxM - 1)$  from initial value 0 ] 1 block A step size setting means to set up the value which took the modulo of  $(NxM - 1)$  about the accumulation value as a new step size at the time of the interleave processing to the following block, A detection means to detect that the counted value of an address count means became  $(NxM - 1)$ , If it is detected that the counted value of an address count means became  $(NxM - 1)$  with this detection means, while memorizing the new step size set up with said step size setting means to the following clock timing a step size output means to output the memorized this step size to an address count means -- since -- it can constitute.

[0036] That is, with the interleave address generation vessel according to claim 2, the value which multiplied the step size which is carrying out the current output by said M is calculated, when only said M batch carries out accumulation of the current step size. In an interleave address generation machine according to claim 1 moreover, a step size operation means While performing the multiplication of the step size according to claim 3 which is carrying out the current output like and said M A step size setting

means to set up the value which took the modulo of  $(NxM - 1)$  about the multiplication value as a new step size at the time of the interleave processing to the following block, A detection means to detect that the counted value of an address count means became  $(NxM - 1)$ , If it is detected that the counted value of an address count means became  $(NxM - 1)$  with this detection means, while memorizing the new step size set up with said step size setting means to the following clock timing a step size output means to output the memorized this step size to an address count means -- since -- it can also constitute.

[0037] That is, with the interleave address generation vessel according to claim 3, the value which multiplied the step size which is carrying out the current output by said  $M$  is calculated by carrying out the multiplication of a current step size and said  $M$ . However, since the direction constituted so that accumulation of the step size according to claim 2 which is carrying out the current output may be carried out  $M$  times like does not need to perform multiplication directly, it is advantageous at the point that circuitry can be simplified.

[0038]

[Embodiment of the Invention] Hereafter, 1 operation gestalt of this invention is explained using a drawing. First, drawing 2 is a block diagram showing the configuration of the interleave address generation machine 1 of the 1st operation gestalt, and drawing 3 is the detailed circuit diagram of the interleave address generation machine 1.

[0039] In addition, the interleave address generation machine 1 of a \*\*\*\* 1 operation gestalt generates read-out in the memory (specifically RAM) which is not illustrated, and the address for writing, in order to perform interleave processing in the  $N$  line  $xM$  train which made 1 block the data of a  $NxM$  individual (however,  $M$  [  $N$  and ] 2 or more integers). Moreover, in the following explanation, Above  $M$  is called "number of columns" which means the number of trains, and the above  $(NxM)$  which is the number of data of 1 block is called "block size."

[0040] As shown in drawing 2, the interleave address generation machine 1 of a \*\*\*\* 1 operation gestalt Count-up actuation is performed from initial value 0 with the step size which synchronizes with a clock from the clock input terminal T1, and is inputted from the exterior. The address counter 3 which outputs the counted value as read-out in memory, and the address for writing, The address outputted from the address counter 3, the data showing the block size -1 ( $= NxM - 1$ ) inputted from the block-size input terminal T2, And based on the data showing the number of columns ( $= M$ ) inputted from number input terminal T3 of columns, it consists of step size computing elements 5 which calculate and output the step size in an address counter 3 synchronizing with the clock from the clock input terminal T1.

[0041] in addition -- an address counter 3 and the step size computing element 5 -- reset-signal input terminal T four -- minding -- a high -- an active reset signal is inputted. Moreover, the data which express the block size -1 ( $= NxM - 1$ ) from the block-size input terminal T2 also with an address counter 3 are inputted. Furthermore, the address is outputted to memory through the address output terminal T5 from an address counter 3.

[0042] As shown in drawing 3, next, an address counter 3 The counted value of the address counter 3 concerned is memorized synchronizing with the clock from the clock input terminal T1. Output the memorized counted value to the address output terminal T5 as the address to memory. The flip-flop group 11 (henceforth the F/F group 11) which consists of a flip-flop with a clock synchronization reset function of the number corresponding to input bus width of face, The adder 13 adding the step size inputted from the output value (namely, address to the memory which is the current counted value of the address counter 3 concerned, and is carrying out the current output) and the step size computing element 5 of the F/F group 11, The subtractor 15 which subtracts the data (only henceforth a block size -1) showing the block size -1 inputted from the block-size input terminal T2 from the result of an operation of the adder 13, The size comparison of the result of an operation of an adder 13 and the block size -1 from the block-size input terminal T2 is carried out. When the result of an operation of an adder 13 is below the block size -1 ( $= NxM - 1$ ) The comparator 17 which outputs a high-level select signal (that is, when the result of an operation of an adder 13 is more than a block size ( $= NxM$ )), otherwise, outputs the select signal of a low level, When the select signal from a comparator 17 is high-level, the result of an operation of an adder 13 is made to input into the data terminal (D) of the F/F group 11. the selector 19

which makes the result of an operation of a subtractor 15 input into the data terminal (D) of the F/F group 11 when the select signal from a comparator 17 is a low level -- since -- it is constituted.

[0043] In addition, the F/F group 11 operates synchronizing with the standup of a clock, and sometimes, the reset signal inputted into the reset terminal (RESET) of self from reset-signal input terminal T four memorizes the data value which is a low level and which is inputted into the data terminal (D) of self through an input bus from a selector 19 to the standup timing of a clock (latch), and usually outputs it to it from an output terminal (Q) to the address output terminal T5. Moreover, irrespective of the output of a selector 19, if a self output value becomes a block size -1 ( $=N \times M - 1$ ), the F/F group 11 consists of standup timing of the following clock so that it may return to 0 the output value of whose is initial value.

[0044] Thus, in the constituted address counter 3, if a high-level reset signal is inputted from reset-signal input terminal T four, the F/F group 11 will be the counted value which is reset synchronizing with the clock from the clock input terminal T1, consequently is memorized by the F/F group 11, and, as for the address outputted to memory, all bits will serve as the initial value 0 of 0 from the address output terminal T5 (refer to drawing 4 ).

[0045] And if the reset signal from reset-signal input terminal T four is set to a low level and reset is canceled, count-up actuation of the address to memory will be performed focusing on the F/F group 11 from the next clock after the reset discharge. As count-up actuation of this address counter 3, the step size inputted from the current output value and the current step size computing element 5 of the F/F group 11 is first added by the adder 13, and the size comparison of the result of an operation of that adder 13 and the value of a block size -1 ( $=N \times M - 1$ ) is carried out by the comparator 17.

[0046] and when the result of an operation of an adder 13 is below the block size -1 ( $=N \times M - 1$ ) By the selector 19 which operates according to the select signal from a comparator 17 The result of an operation of an adder 13 is inputted into the data terminal (D) of the F/F group 11 as it is. Consequently, the F/F group 11 While memorizing the result of an operation of an adder 13 as counted value of the address counter 3 concerned to the standup timing of the following clock, the memorized counted value will be outputted to the address output terminal T5 as the address to memory from a self output terminal (Q).

[0047] moreover, conversely, when the result of an operation of an adder 13 is more than a block size ( $=N \times M$ ) By the above-mentioned selector 19, the value which is the result of an operation of a subtractor 15, and subtracted the block size -1 ( $=N \times M - 1$ ) from the result of an operation of an adder 13 It is inputted into the data terminal (D) of the F/F group 11. Consequently, the F/F group 11 While memorizing the result of an operation of a subtractor 15 as counted value of the address counter 3 concerned to the standup timing of the following clock, the memorized counted value will be outputted to the address output terminal T5 as the address to memory from a self output terminal (Q).

[0048] Therefore, although count-up actuation will be performed from initial value 0 with the step size which synchronizes with a clock and is inputted from the step size computing element 5 according to an operation of the F/F group 11 and an adder 13 and the counted value will be outputted as the address to memory in an address counter 3 When the counted value in the following clock timing becomes more than a block size ( $=N \times M$ ) especially The value which took the modulo of a block size -1 ( $=N \times M - 1$ ) about the value more than the block size turns into counted value in the following clock timing according to an operation of a subtractor 15, a comparator 17, and a selector 19. And when the counted value in further this clock timing becomes a block size -1 ( $=N \times M - 1$ ), the counted value in the following clock timing will return to initial value 0 according to the operation of the F/F group 11 mentioned above.

[0049] As shown in drawing 3 , on the other hand, the step size computing element 5 An address counter 3 memorizes the step size used for the above-mentioned count-up actuation synchronizing with the clock from the clock input terminal T1. It is an address counter 3 (in detail) about the memorized step size. The flip-flop with [ 1st bit ] a clock synchronization preset feature outputted to the adder 13 of an address counter 3, The flip-flop group 21 (henceforth the F/F group 21) which except [ its ] becomes from a flip-flop with a clock synchronization reset function, The operation value produced from the F/F

group 21 in the process in which the step size which should be outputted to an address counter 3 is calculated. It has the flip-flop group 23 (henceforth the F/F group 23) which consists of a number corresponding to input bus width of face of flip-flops with a clock synchronization reset function memorized synchronizing with the clock from the clock input terminal T1.

[0050] In addition, the F/F groups 21 and 23 operate synchronizing with the standup of a clock, and sometimes, the signal inputted into self reset terminal (RESET) or presetting terminal (SET) memorizes the data value which is a low level and which is inputted into the data terminal (D) of self through an input bus to the standup timing of a clock (latch), and usually outputs them to it from an output terminal (Q). Moreover, the adder 25 with which the step size computing element 5 adds the output value (namely, step size which is carrying out the current output from the F/F group 21 to the address counter 3) of the F/F group 21, and the output value of the F/F group 23. The subtractor 27 which subtracts the block size -1 ( $=N \times M - 1$ ) inputted from the block-size input terminal T2 from the result of an operation of the adder 25. The size comparison of the result of an operation of an adder 25 and the block size -1 from the block-size input terminal T2 is carried out. When the result of an operation of an adder 25 is below the block size -1 ( $=N \times M - 1$ ) The comparator 29 which outputs a high-level select signal (that is, when the result of an operation of an adder 25 is more than a block size ( $=N \times M$ )), otherwise, outputs the select signal of a low level. When the select signal from a comparator 29 is high-level, the result of an operation of an adder 25 is chosen and outputted. The selector 31 which chooses and outputs the result of an operation of a subtractor 27 when the select signal from a comparator 29 is a low level. Data showing the number of columns inputted from the counted value (namely, address currently outputted to memory from the F/F group 11 of an address counter 3) of an address counter 3, and number input terminal T3 of columns (only below) A size comparison is carried out. the number of columns -- saying, when the counted value of an address counter 3 is smaller than the number of columns ( $=M$ ) The comparator 33 which outputs a high-level select signal (that is, when the counted value of an address counter 3 is more than the number of columns ( $=M$ )), otherwise, outputs the select signal of a low level. When the select signal from a comparator 33 is high-level, the output of a selector 31 is made to input into the data terminal (D) of the F/F group 23. When the select signal from a comparator 33 is a low level, it has the selector 35 which makes the output of the F/F group 23 input into the data terminal (D) of this F/F group 23.

[0051] And the step size computing element 5 compares the counted value of an address counter 3 with the block size -1 from the block-size input terminal T2 further. When the counted value of an address counter 3 is equal to a block size -1 ( $=N \times M - 1$ ) The comparator 37 which outputs a high-level select signal (that is, when the counted value of an address counter 3 is not equal to a block size -1 ( $=N \times M - 1$ )), otherwise, outputs the select signal of a low level. When the select signal from a comparator 37 is high-level, the output of the F/F group 23 is made to input into the data terminal (D) of the F/F group 21. The selector 39 which makes the output of the F/F group 21 input into the data terminal (D) of this F/F group 21 when the select signal from a comparator 37 is a low level. It has OR circuit 41 which makes the OR signal of the reset signal from reset-signal input terminal T four, and the select signal from a comparator 37 input into the reset terminal (RESET) of the F/F group 23.

[0052] Next, actuation of the step size computing element 5 constituted as mentioned above is explained. First, if a high-level reset signal is inputted from reset-signal input terminal T four, by the F/F group 23, the signal inputted into the reset terminal (RESET) of each of that flip-flop will become high-level through OR circuit 41, and will become high-level [ the signal inputted into the presetting terminal (SET) of the bit / 1st / flip-flop, and the reset terminal (RESET) of the flip-flop of the other bit, respectively ] in the F/F group 21.

[0053] For this reason, if a high-level reset signal is inputted from reset-signal input terminal T four, as for the output value of the F/F group 23, all bits will be set to 0 synchronizing with the clock from the clock input terminal T1. Moreover, the step size which the 1st bit is 1, and the other bit is set to 0 by the output value of the F/F group 21, consequently is outputted to an address counter 3 is set to 1 as initial value (refer to drawing 4 ).

[0054] Then, if the reset signal from reset-signal input terminal T four is set to a low level and reset is

canceled, the F/F group 23 will latch and output the output of the selector 35 which operates according to the select signal from a comparator 33 synchronizing with a clock.

[0055] A selector 35 makes the output of a selector 31 input into the data terminal (D) of the F/F group 23 here (namely, when for the address which is the counted value of an address counter 3 and is outputted from the address output terminal T5 to be smaller than the number of columns ( $=M$ )), when the select signal from a comparator 33 is high-level.

[0056] And a selector 31 follows a select signal from a comparator 29. The result of an operation to which the output value of the F/F group 21 and the output value of the F/F group 23 were added by the adder 25 In being below the block size -1 ( $=N \times M - 1$ ) from the block-size input terminal T2 Output the result of an operation of the adder 25 to a selector 35 as it is, and conversely, when the result of an operation of an adder 25 is more than the block count ( $=N \times M$ ) The result of an operation by which the block size -1 ( $=N \times M - 1$ ) was subtracted from the result of an operation of an adder 25 with the subtractor 27 is outputted to a selector 35.

[0057] Moreover, a selector 35 makes the output of the F/F group 23 input into the data terminal (D) of the F/F group 23 (namely, when it to be the present counted value of an address counter 3 and for the address currently outputted from the address output terminal T5 to be more than the number of columns ( $=M$ )), when the select signal from a comparator 33 is a low level.

[0058] therefore, when the counted value of an address counter 3 is smaller than the number of columns ( $=M$ ), the F/F group 23 The value which took the modulo of a block size -1 ( $=N \times M - 1$ ) about the value adding a self current output value and the output value of the F/F group 23 It will hold without latching to the following clock timing, and updating a self output value, when the counted value of an address counter 3 is more than the number of columns ( $=M$ ).

[0059] The F/F group 23 consequently, by operating in collaboration with an adder 25, a subtractor 27, comparators 29 and 33, and selectors 31 and 35 While only column several M batches carry out accumulation of the step size currently outputted from the F/F group 21 during the period for [ until the counted value of an address counter 3 serves as a block size -1 ( $=N \times M - 1$ ) from initial value 0 ] 1 block The value which took the modulo of a block size -1 ( $=N \times M - 1$ ) about the accumulation value will be memorized as a new step size at the time of the interleave processing to the following block. And the value which took the modulo of a block size -1 ( $=N \times M - 1$ ) by this actuation about the value which multiplied the step size which is carrying out the current output to the address counter 3 by the number of columns ( $=M$ ) is set up as a new step size at the time of the interleave processing to the following block.

[0060] Moreover, if the counted value of an address counter 3 becomes a block size -1 ( $=N \times M - 1$ ), a comparator 37 will judge that it is the last entry-of-data timing of a block, and will output a high-level select signal. And the high-level select signal from the comparator 37 is inputted into the reset terminal (RESET) of the F/F group 23 through OR circuit 41. Therefore, the F/F group 23 will be reset to the following clock timing (namely, timing which the counted value of an address counter 3 is the timing which returns to initial value 0, and inputs the data of the beginning of the following block), and the output value will return to 0. That is, the high-level select signal outputted from a comparator 37 is an end-of-block signal meaning 1-block termination.

[0061] On the other hand, if the reset signal from reset-signal input terminal T four is set to a low level from high level and reset is canceled in the step size computing element 5 concerned, the F/F group 21 will latch the output of the selector 39 which operates according to the select signal from a comparator 37 synchronizing with a clock, and will output it as a step size.

[0062] When the select signal from a comparator 37 of a selector 39 is a low level here Namely, (when the counted value of an address counter 3 is not a block size -1 ( $=N \times M - 1$ )) The output of the F/F group 21 is made to input into the data terminal (D) of the F/F group 21. Moreover, when the select signal from a comparator 37 is high-level, the output of the F/F group 23 is made to input into the data terminal (D) of the F/F group 21 (namely, when for the counted value of an address counter 3 to be a block size -1 ( $=N \times M - 1$ )).

[0063] Therefore, the F/F group 21 is the following clock timing (namely, timing from which the

counted value of an address counter 3 returns to initial value 0), when the counted value of an address counter 3 becomes a block size -1 ( $=N \times M - 1$ ). The new step size to the following block memorized by the F/F group 23 just before that is latched. The latched step size will be outputted to an address counter 3 during the period for [ until the counted value of an address counter 3 returns from a block size -1 ( $=N \times M - 1$ ) to initial value 0 next ] 1 block.

[0064] That is, the F/F group 21 will output the memorized new step size to an address counter 3, while memorizing the new step size latched to the F/F group 23 to the following clock timing, if it is detected that the counted value of an address counter 3 became a block size -1 ( $=N \times M - 1$ ) with the comparator 37 by operating in collaboration with a selector 39. And the step size with which the counted value of an address counter 3 is outputted to that address counter 3 by this actuation synchronizing with the timing which returned to initial value 0 is changed into a new step size.

[0065] Next, drawing 4 is a timing diagram which mentions as an example the case where the interleave address generation machine 1 mentioned above is operated in interleave processing with a block size with a line count (low number)  $N=4$  and  $M=3$  trains (the number of columns), and expresses it. In addition, when the interleave address generation machine 1 of this operation gestalt is used, synchronizing with the clock to the clock input terminal T1, the sequential input of the data is carried out to memory.

[0066] The period which inputs the data (D 1-1 - D 1-12) of the 1st block in the case of this example as shown in drawing 4 In (namely, the period for 12 periods of the clock which is equivalent to 1 block of data from from just before a reset signal changes from high level to a low level) From an address counter 3, the address will be outputted in order of 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11. This is because the initial value of the step size outputted from the F/F group 21 of the step size computing element 5 is 1.

[0067] According to moreover, an operation of the circuit part which consists of the F/F group 23 of the step size computing element 5, an adder 25, a subtractor 27, comparators 29 and 33, and selectors 31 and 35 in this period While accumulation of the step size ( $=1$ ) by which the current output is carried out from the F/F group 21 is carried out at each \*\*\*\* of 0, 1, and 2 with the address smaller than the number M of columns ( $=3$ ) from an address counter 3 The value ( $=3$ ) which took the modulo of a block size -1 ( $=11$ ) about the accumulation value is memorized by the F/F group 23 as a new step size to the following block. In addition, since it does not become more than a block size ( $=12$ ) in this case even if it carries out accumulation of the step size 3 times, the value memorized by the F/F group 23 changes with  $0 \rightarrow 1 \rightarrow 2 \rightarrow 3$ .

[0068] When the address outputted from an address counter 3 returns to 0 from 11, and to the timing While the new step size ( $=3$ ) memorized by the F/F group 23 is latched to the F/F group 21 The new step size ( $=3$ ) with which the output value of the F/F group 23 was latched to 0 by return and the F/F group 21 will be outputted to an address counter 3 as a step size in the period which inputs the data (D 2-1 - D 2-12) of the 2nd block.

[0069] For this reason, in the period which inputs the data (D 2-1 - D 2-12) of the 2nd block, the address will be outputted from an address counter 3 in order of 0, 3, 6, 9, 1, 4, 7, 10, 2, 5, 8, and 11. That in addition, the address outputted is changing to the degree of 9 in this period 1 Since the value ( $=12$ ) which added 3 which is a current step size to 9 becomes more than a block size ( $=12$ ), in this case 1 which is the result of an operation of a subtractor 15, and is the value which took the modulo of a block size -1 ( $=11$ ) about 12 is because it is latched to the F/F group 11 as following counted value. And this is the same also about the case where the address outputted changes to the degree of 10 2.

[0070] According to moreover, an operation of the circuit part which consists of the F/F group 23 of the step size computing element 5, an adder 25, a subtractor 27, comparators 29 and 33, and selectors 31 and 35 in this period While accumulation of the step size ( $=3$ ) by which the current output is carried out from the F/F group 21 is carried out at each \*\*\*\* of 0, 1, and 2 with the address smaller than the number M of columns ( $=3$ ) from an address counter 3 The value ( $=9$ ) which took the modulo of a block size -1 ( $=11$ ) about the accumulation value is memorized by the F/F group 23 as a new step size to the following block. In addition, since it does not become more than a block size ( $=12$ ) in this case even if

it carries out accumulation of the step size 3 times, the value memorized by the F/F group 23 changes with 0->3->6->9.

[0071] When the address outputted from an address counter 3 returns to 0 from 11, and to the timing While the new step size (= 9) memorized by the F/F group 23 is latched to the F/F group 21 The new step size (= 9) with which the output value of the F/F group 23 was latched to 0 by return and the F/F group 21 will be outputted to an address counter 3 as a step size in the period which inputs the data (D 3-1 - D 3-12) of the 3rd block.

[0072] For this reason, in the period which inputs the data (D 3-1 - D 3-12) of the 3rd block, the address will be outputted from an address counter 3 in order of 0, 9, 7, 5, 3, 1, 10, 8, 6, 4, 2, and 11. That in addition, the address outputted is changing to the degree of 9 in this period 7 Since the value (= 18) which added 9 which is a current step size to 9 becomes more than a block size (= 12), in this case 7 which is the result of an operation of a subtractor 15, and is the value which took the modulo of a block size -1 (= 11) about 18 is because it is latched to the F/F group 11 as following counted value. And this is the same also about the case where the address outputted changes to the degree of 7 5, and the case where it changes to the degree of 5 3.

[0073] According to moreover, an operation of the circuit part which consists of the F/F group 23 of the step size computing element 5, an adder 25, a subtractor 27, comparators 29 and 33, and selectors 31 and 35 in this period While accumulation of the step size (= 9) by which the current output is carried out from the F/F group 21 is carried out at each \*\*\*\* of 0, 1, and 2 with the address smaller than the number M of columns (= 3) from an address counter 3 The value (= 5) which took the modulo of a block size -1 (= 11) about the accumulation value is memorized by the F/F group 23 as a new step size to the following block. In addition, the value memorized by the F/F group 23 in this case changes with 0->9->7->5.

[0074] Although not shown in drawing 4, when the address outputted from an address counter 3 returns to 0 from 11 after that, and to the timing While the new step size (= 5) memorized by the F/F group 23 is latched to the F/F group 21 The new step size (= 5) with which the output value of the F/F group 23 was latched to 0 by return and the F/F group 21 will be outputted to an address counter 3 as a step size in the period which inputs the data of the 4th block. For this reason, in the period which inputs the data of the 4th block, the address will be outputted from an address counter 3 in order of 0, 5, 10, 4, 9, 3, 8, 2, 7, 1, 6, and 11.

[0075] as mentioned above, with the interleave address generation vessel 1 of a \*\*\*\* 1 operation gestalt, whenever the address outputted returns from a block size -1 (=  $N \times M - 1$ ) to initial value 0, it will come out, and there will be a step size of the address outputted from an address counter 3 synchronizing with a clock, and it will be changed by the step size computing element 5 for every 1 block of input data.

[0076] Therefore, according to this interleave address generation machine 1, it sets at the period which inputs the data of the 1st block. In the period which inputs the data of each block of input data of sequential writing and the 2nd henceforth into each address of the memory outputted from an address counter 3 While reading data from each address of the memory outputted from an address counter 3 By overwriting the present input data to the read address, as mentioned already using drawing 1, addressing of the read-out of the data from memory will be carried out with a different step size from the time of writing in the data. For example, in the case of the example shown in drawing 4, supposing it attaches to order D1, D2, D3, D4, D5, D6, D7, D8, D9, and an index called D10, D11, and D12 from the 1st thing to the input data for 1 block The input data of each block by which a sequential input is carried out will be rearranged into the sequence of D1, D4, D7, D10 and D2, D5, D8, D11 and D3, D6, D9, and D12 by being read from memory, respectively.

[0077] For this reason, according to the interleave address generation machine 1 of a \*\*\*\* 1 operation gestalt, only by having 1 set of of the interleave address generation machine 1 concerned and memory, the continuous interleave processing to the data of two or more blocks is attained, and the circuit (interleave circuit) for performing interleave processing can be miniaturized.

[0078] In addition, with the \*\*\*\* 1 operation gestalt, the address counter 3 is equivalent to the address count means, and actuation of the address counter 3 is equivalent to address count processing. Moreover,

the step size computing element 5 is equivalent to the step size operation means, and actuation of the step size computing element 5 is equivalent to step size setting processing. And among each part which constitutes the step size computing element 5, the F/F group 23, an adder 25, a subtractor 27, comparators 29 and 33, selectors 31 and 35, and OR circuit 41 are equivalent to a step size setting means according to claim 2, a comparator 37 is equivalent to a detection means according to claim 2, and the F/F group 21 and the selector 39 are equivalent to the step size output means according to claim 2.

[0079] By the way, although the value which multiplied the step size which is carrying out the current output to the address counter 3 by the number M of columns was calculated with the interleave address generation vessel 1 of the above-mentioned 1st operation gestalt when only column several M batches carried out accumulation of the current step size, it may be made to carry out the direct multiplication of a current step size and the number M of columns.

[0080] then -- next, a current step size -- several columns -- the value which multiplied by M -- a current step size and several columns -- the interleave address generation machine of the 2nd operation gestalt for which it asked by carrying out the multiplication of M with a multiplier is explained concretely. First, drawing 5 is a circuit diagram showing the interleave address generation machine 43 of a \*\*\*\* 2 operation gestalt. In addition, in drawing 5, about the same component as the interleave address generation machine 1 of the 1st operation gestalt mentioned above, since the same sign is attached, detailed explanation is omitted.

[0081] As shown in drawing 5, as compared with the interleave address generation machine 1 of the 1st operation gestalt, only the configurations of the step size computing element 45 differ, and the address counter 3 of the interleave address generation machine 43 of a \*\*\*\* 2 operation gestalt is completely the same. And the step size computing element 45 of a \*\*\*\* 2 operation gestalt It compares with the step size computing element 5 of the 1st operation gestalt. Instead of an adder 25, a subtractor 27, comparators 29 and 33, selectors 31 and 35, and OR circuit 41 The multiplier 47 which carries out the multiplication of the output value (namely, current step size) of the F/F group 21, and the number of columns from number input terminal T3 of columns (=M), When the counted value (namely, address currently outputted to memory from the F/F group 11 of an address counter 3) of an address counter 3 is 0 The comparator 49 which outputs a high-level select signal, and outputs the select signal of a low level when the counted value of an address counter 3 is not 0, The selector 51 which chooses and outputs the result of an operation of a multiplier 47 when the select signal from a comparator 49 is high-level, and chooses and outputs the output of the F/F group 23 when the select signal from a comparator 49 is a low level, The subtractor 53 which subtracts the block size -1 (=NxM -1) inputted from the block-size input terminal T2 from the output of the selector 51, The size comparison of the output of a selector 51 and the block size -1 from the block-size input terminal T2 is carried out. When the output of a selector 51 is below the block size -1 (=NxM -1) The comparator 55 which outputs a high-level select signal (that is, when the output of a selector 51 is more than a block size (=NxM)), otherwise, outputs the select signal of a low level, When the select signal from a comparator 55 is high-level, the output of a selector 51 is made to input into the data terminal (D) of the F/F group 23. When the select signal from a comparator 55 is a low level, it has the selector 57 which makes the result of an operation of a subtractor 53 input into the data terminal (D) of the F/F group 23.

[0082] And in this step size computing element 45, the direct input of the reset signal from reset-signal input terminal T four is carried out to the reset terminal (RESET) of the F/F group 23. Thus, in the constituted step size computing element 45, if a high-level reset signal is inputted from reset-signal input terminal T four, by the F/F group 23, the signal inputted into the reset terminal (RESET) of each of that flip-flop will become high-level, and the signal inputted into the presetting terminal (SET) of the bit [ 1st ] flip-flop and the reset terminal (RESET) of the flip-flop of the other bit, respectively will become high-level by the F/F group 21.

[0083] For this reason, like the step size computing element 5 of the 1st operation gestalt, if a high-level reset signal is inputted from reset-signal input terminal T four, as for the output value of the F/F group 23, all bits will be set to 0 synchronizing with the clock from the clock input terminal T1. Moreover, the step size which the 1st bit is 1, and the other bit is set to 0 by the output value of the F/F group 21,

consequently is outputted to an address counter 3 is set to 1 as initial value (refer to drawing 6 ).

[0084] And if the reset signal from reset-signal input terminal T four is set to a low level and reset is canceled after that, the F/F group 23 will latch and output the output of a selector 57 synchronizing with a clock. It sets to the step size computing element 45 of a \*\*\*\* 2 operation gestalt here. When the counted value of an address counter 3 is 0, from a selector 51 The multiplication result to which the multiplication of the output value and the number of columns ( $=M$ ) of the F/F group 21 was carried out by the multiplier 47 is outputted, and further, if the multiplication result of the multiplier 47 is below the block size -1 ( $=N \times M - 1$ ) The multiplication result is outputted to the data terminal (D) of the F/F group 23 from a selector 57 as it is, and with [ the result of an operation of a multiplier 47 ] the block count [ more than ] ( $=N \times M$ ), conversely The result of an operation by which the block size -1 ( $=N \times M - 1$ ) was subtracted from the multiplication result of a multiplier 47 with the subtractor 53 is outputted to the data terminal (D) of the F/F group 23 from a selector 57.

[0085] moreover, when the counted value of an address counter 3 is not 0 The direction of the output of the F/F group 23 is chosen and outputted from a selector 51, and further, if the output value of the F/F group 23 is below the block size -1 ( $=N \times M - 1$ ) The output of the F/F group 23 is outputted to the data terminal (D) of the F/F group 23 from a selector 57 as it is, and with [ the output value of the F/F group 23 ] the block count [ more than ] ( $=N \times M$ ), conversely The result of an operation by which the block size -1 ( $=N \times M - 1$ ) was subtracted from the output value of the F/F group 23 with the subtractor 53 is outputted to the data terminal (D) of the F/F group 23 from a selector 57.

[0086] For this reason, the F/F group 23 will memorize the value which took the modulo of a block size -1 ( $=N \times M - 1$ ) about the multiplication value which carried out the multiplication of the step size currently outputted from the F/F group 21, and the number M of columns as a new step size at the time of the interleave processing to the following block by operating in collaboration with a multiplier 47, a subtractor 53, comparators 49 and 55, and selectors 51 and 57. And the value which took the modulo of a block size -1 ( $=N \times M - 1$ ) by this actuation about the value which multiplied the step size which is carrying out the current output to the address counter 3 by the number of columns ( $=M$ ) is set up as a new step size at the time of the interleave processing to the following block.

[0087] On the other hand, if the reset signal from reset-signal input terminal T four is set to a low level from high level and reset is canceled like the step size computing element 5 of the 1st operation gestalt also in the step size computing element 45 concerned, the F/F group 21 will latch the output of the selector 39 which operates according to the select signal from a comparator 37 synchronizing with a clock, and will output it as a step size. And when the select signal from a comparator 37 of a selector 39 is a low level Namely, (when the counted value of an address counter 3 is not a block size -1 ( $=N \times M - 1$ )) The output of the F/F group 21 is made to input into the data terminal (D) of the F/F group 21. Moreover, when the select signal from a comparator 37 is high-level, the output of the F/F group 23 is made to input into the data terminal (D) of the F/F group 21 (namely, when for the counted value of an address counter 3 to be a block size -1 ( $=N \times M - 1$ )).

[0088] Also in the step size computing element 45 of a \*\*\*\* 2 operation gestalt therefore, the F/F group 21 When the counted value of an address counter 3 becomes a block size -1 ( $=N \times M - 1$ ), to the following clock timing (namely, timing from which the counted value of an address counter 3 returns to initial value 0) The new step size to the following block memorized by the F/F group 23 is latched. The latched step size will be outputted to an address counter 3 during the period for [ until the counted value of an address counter 3 returns from a block size -1 ( $=N \times M - 1$ ) to initial value 0 next ] 1 block.

[0089] Here, drawing 6 is a timing diagram which mentions as an example the case where operate the interleave address generation machine 43 of a \*\*\*\* 2 operation gestalt, and it operates interleave processing with a block size with a line count (low number)  $N=4$  and  $M=3$  trains (the number of columns), and expresses it. As shown in drawing 6 , and with the interleave address generation vessel 43 of a \*\*\*\* 2 operation gestalt In initiation of a period to the 2nd clock timing to input [ of the F/F group 23 ] the data (D 1-1 - D 1-12) of the 1st block In initiation of a period to the 2nd clock timing which changes to 0-3 and inputs the data (D 2-1 - D 2-12) of the 2nd block In initiation of a period to the 2nd, and each 3rd clock timing which changes to 9 from 3 and inputs the data (D 3-1 - D 3-12) of the 3rd

block further Only the point which carries out sequential change with 9->16->5 differs from the interleave address generation machine 1 of the 1st operation gestalt.

[0090] And also with such an interleave address generation vessel 43 of a \*\*\*\* 2 operation gestalt, the address will be outputted in the completely same sequence as the interleave address generation machine 1 of the 1st operation gestalt, it only has 1 set of of the interleave address generation machine 43 concerned and memory, and the continuous interleave processing to the data of two or more blocks is attained from an address counter 3.

[0091] In addition, with the \*\*\*\* 2 operation gestalt, the address counter 3 is equivalent to the address count means, and actuation of the address counter 3 is equivalent to address count processing. Moreover, the step size computing element 45 is equivalent to the step size operation means, and actuation of the step size computing element 45 is equivalent to step size setting processing. And among each part which constitutes the step size computing element 45, the F/F group 23, a multiplier 47, a subtractor 53, comparators 49 and 55, and selectors 51 and 57 are equivalent to a step size setting means according to claim 3, a comparator 37 is equivalent to a detection means according to claim 3, and the F/F group 21 and the selector 39 are equivalent to the step size output means according to claim 3.

[0092] As mentioned above, although 1 operation gestalt of this invention was explained, it cannot be overemphasized that this invention is not limited to the operation gestalt mentioned above, and various gestalten can be taken. For example, although the initial value of the step size outputted to an address counter 3 from the step size computing elements 5 and 45 was 1 with each operation gestalt mentioned above, the initial value of a step size should just be one or more integers.

[0093] Moreover, what is necessary is to add the value of the start address of memory to the address outputted from an address counter 3, and just to make it supply the address after the addition to it at the address input terminal of memory, when the number of the start addresses of the memory used for interleave processing is not zero.

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[Translation done.]

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## TECHNICAL PROBLEM

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[Problem(s) to be Solved by the Invention] By the way, in the above-mentioned conventional interleave circuit 101, it is necessary to hold the data for 1 block until it finishes data read-out from RAM103. therefore, in order to carry out interleave processing of the data of two or more blocks by which a sequential input is carried out continuously Two circuit blocks 101A and 101B which have the same configuration as the interleave circuit 101 of drawing 7 as shown in drawing 9, The delay circuit 109 which delays by 1 block that a clock begins to be supplied to one circuit block 101B, The most significant bit Qn of the address counter 105 in circuit block 101A of another side When it is "1" The data outputted from the data output terminal DOUT of circuit block 101A are outputted as output data, and it is the above-mentioned most significant bit Qn conversely. In being "0" From the selector 111 outputted as output data, the data outputted from the data output terminal DOUT of circuit block 101B An interleave circuit is constituted and it is necessary to make it each of the circuit blocks 101A and 101B take charge of the phase which writes data in RAM103, and the phase which reads data from RAM103 by turns to timing as shown in drawing 10.

[0014] In addition, drawing 10 shows the case where interleave processing is performed having used 4x4 data as 1 block, like drawing 8. And it sets to drawing 10 and is Qn. For the output data to 1-16, and a number, interleave processing is carried out by circuit block 101A, and the number currently outputted when it is "1" is [ 33 or more output data ] Qn. When it is "0", as for the output data to 17-32, interleave processing of the number currently outputted is carried out by circuit block 101B.

[0015] Thus, in the Prior art, in order to perform interleave processing continuously to the data of two or more blocks by which a sequential input is carried out, it was difficult to miniaturize the circuit for forming the interleave address generation machine which consists of an address counter 105 and an address selector 107, and every two RAM103, and performing interleave processing. And since especially interleave processing of this kind is carried out with mobile communication equipment etc., it is required that the circuit which performs interleave processing should be small.

[0016] Then, this invention aims at offering the interleave address generation machine and the interleave address generation approach of carrying out continuous interleave processing to the data of two or more blocks by one memory.

[0017]

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## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is an explanatory view explaining an operation of this invention.

[Drawing 2] It is a block diagram showing the configuration of the interleave address generation machine of the 1st operation gestalt.

[Drawing 3] It is a circuit diagram showing the configuration of the interleave address generation machine of the 1st operation gestalt.

[Drawing 4] It is a timing diagram showing actuation of the interleave address generation machine of drawing 3.

[Drawing 5] It is a circuit diagram showing the configuration of the interleave address generation machine of the 2nd operation gestalt.

[Drawing 6] It is a timing diagram showing actuation of the interleave address generation machine of drawing 5.

[Drawing 7] It is a block diagram showing the basic configuration of the interleave circuit using the conventional interleave address generation machine.

[Drawing 8] It is an explanatory view explaining actuation of the interleave circuit of drawing 7.

[Drawing 9] It is a block diagram showing the configuration of the conventional interleave circuit for carrying out interleave processing of the data of two or more blocks continuously.

[Drawing 10] It is a timing diagram showing actuation of the interleave circuit of drawing 9.

[Description of Notations]

1 43 -- Interleave address generation machine

3 -- Address counter 5 45 -- Step size computing element

11, 21, 23 -- Flip-flop group (F/F group)

13 25 -- Adder 15, 27, 53 -- Subtractor 47 -- Multiplier

17, 29, 33, 37, 49, 55 -- Comparator

19, 31, 35, 39, 51, 57 -- Selector 41 -- OR circuit

T1 -- Clock input terminal T2 -- Block-size input terminal

T3 -- The number input terminal of columns T four -- Reset-signal input terminal

T5 -- Address output terminal

[Translation done.]

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**TECHNICAL FIELD**

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[Field of the Invention] Especially this invention relates to the interleave processing for reducing the effect of the burst error in a digital communication system about a digital-communication technique.  
[0002]

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## PRIOR ART

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[Description of the Prior Art] Generally, big effectiveness is not acquired even if it applies the error correction processing by the Viterbi decoder, the Lead Solomon decoder, etc. directly to the data transmitted on a radio-transmission way, since error data generate intensively the burst error generated in the radio-transmission on the street of a digital communication system.

[0003] Then, the concentrated error data based on an burst error are distributed, and he changes into a random error, and is trying for this to aim at an improvement of the error correction effectiveness by using interleave processing together with error correction processing to the data transmitted on a radio-transmission way conventionally.

[0004] He replaces the sequence of data and is trying to transmit by the transmitting side in this interleave processing. And data are returned in order of origin by performing actuation contrary to a transmitting side by the receiving side. Since the burst error in a transmission line is distributed and it is changed into a random error by carrying out like this, the error correction effectiveness can be heightened.

[0005] Here, in such interleave processing, in order to replace the sequence of the data which make 1 block  $N \times M$  piece (however,  $M$  [  $N$  and ] 2 or more integers), there is a method of using RAM (random access memory). and he performs X-Y conversion with an imagination line address and the train address, and is trying to output input data in different sequence from the sequence at the time of an input by this approach by writing input data in RAM in order of that line address, assuming that it is what has the line address of  $N$  line, and the train address of  $M$  train in RAM, and reading data from RAM in order of the train address after that write-in termination

[0006] As shown in drawing 7, for example, the conventional interleave circuit 101 which performs such interleave processing RAM103 which outputs the stored data from the data output terminal DOUT while storing the input data from the data input terminal DIN, the  $n+1$ -bit address counter 105 which performs count-up actuation every [ 1 ] from initial value 0 synchronizing with the clock from the clock input terminal CLK -- and  $n+1$ -bit data  $Q_0$  - $Q_n$  outputted from an address counter 105 In inside the most significant bit  $Q_n$   $n$  bit-data  $Q_0$  - $Q_{n-1}$  of an except the 1st for  $n$  bits -- input terminal  $a_0$  - $a_{n-1}$  While being inputted above-mentioned  $n$  bit-data  $Q_0$  - $Q_{n-1}$  from an address counter 105 Low order  $m$  bit  $Q_0$  - $Q_{m-1}$  which can be set High order  $(n-m)$  bit  $Q_m$  - $Q_{n-1}$   $n$  bit-data  $Q_m$  - $Q_{n-1}$  replaced and  $Q_0$  - $Q_{m-1}$  the 2nd for  $n$  bits -- input terminal  $b_0$  - $b_{n-1}$  It has the interleave address generation machine which consists of an inputted address selector 107.

[0007] And an address selector 107 is the most significant bit  $Q_n$  of an address counter 105. For example, in being "0" the 1st -- input terminal  $a_0$  - $a_{n-1}$  Data  $Q_0$  - $Q_{n-1}$  from the address counter 105 inputted output terminal  $Y_0$  - $Y_{n-1}$  of self from -- address input terminal  $A_0$  - $A_{n-1}$  of RAM103 Write in and it outputs as the address. On the contrary, the most significant bit  $Q_n$  of an address counter 105 In being "1" the 2nd -- input terminal  $b_0$  - $b_{n-1}$  Data  $Q_m$  - $Q_{n-1}$  from the address counter 105 inputted, and  $Q_0$  - $Q_{m-1}$  Output terminal  $Y_0$  - $Y_{n-1}$  of self from -- address input terminal  $A_0$  - $A_{n-1}$  of RAM103 It reads and outputs as the address.

[0008] And RAM103 is the most significant bit  $Q_n$  of an address counter 105 further. In being "0" The

data by which a sequential input is carried out from the data input terminal DIN synchronizing with a clock Address input terminal A0 -An-1 It stores in the address shown with the data inputted, and is the most significant bit Qn of an address counter 105. In being "1" Address input terminal A0 -An-1 Synchronizing with a clock, the sequential output of the data of the address shown with the data inputted is carried out from the data output terminal DOUT.

[0009] When writing input data in RAM103 in such an interleave circuit 101, it is n bit-data Q0 -Qn-1 from an address counter 105 by the address selector 107. It is address input terminal A0 -An-1 of RAM103 as it is. Since it writes in and is outputted as the address, data will be written in sequentially from the 0th street of RAM103.

[0010] moreover, in reading data from RAM103 an address selector 107 -- n bit-data Q0 -Qn-1 from an address counter 105 Low order m bit Q0 -Qm-1 which can be set High order (n-m) bit Qm -Qn-1 n bit-data Qm -Qn-1 replaced and Q0 -Qm-1 Address input terminal A0 -An-1 of RAM103 Since it reads and is outputted as the address, data will be read in the sequence which replaced the line address and the train address of RAM103 to the time of the writing of data.

[0011] For example, when interleave processing in four line x4 train is performed, the input data from the data input terminal DIN will be written in RAM103 in order of the address shown in drawing 8 (A) (namely, when interleave processing is performed having used 4x4 data as 1 block). And when all the data of 16 (= 4x4) individual for 1 block are written in next, data will be read from RAM103 in order of the address shown in drawing 8 (B), and the sequential output of the read data will be carried out from the data output terminal DOUT. In addition, the number in O in drawing 8 (A) shows the sequence of the address which writes in data, and the number in \*\* in drawing 8 (B) shows the sequence of the address which reads data.

[0012] Therefore, supposing it attaches D1, D2 and D3, --, an index called D14, D15, and D16 sequentially from the 1st thing to the input data for 1 block From the data output terminal DOUT, input data will be rearranged and outputted to D1, D5, D9, D13 and D2, D6, D10, D14 and D3, D7, D11, D15 and D4, D8, and order called D12 and D16.

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[Translation done.]

JAPANESE

[JP,2000-078030,A]

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CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE  
INVENTION TECHNICAL PROBLEM DESCRIPTION OF DRAWINGS DRAWINGS

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CLAIMS

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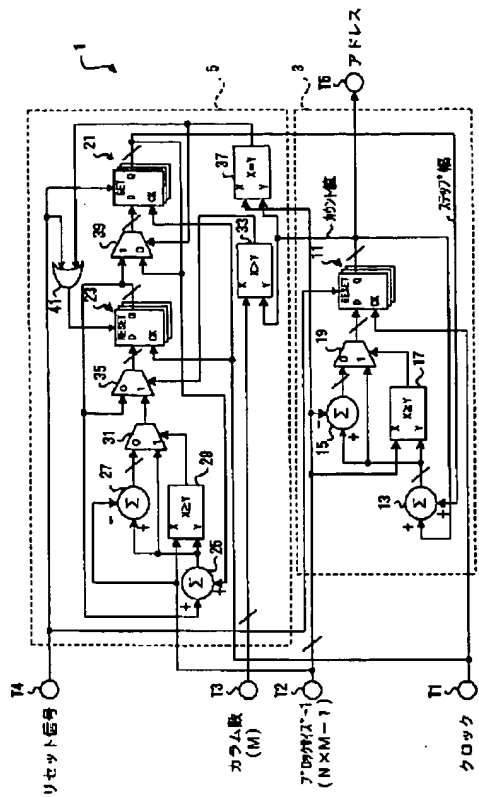
[Claim(s)]

[Claim 1] While carrying out the sequential input of the data which make 1 block a  $N \times M$  individual (however,  $M$  [  $N$  and ] 2 or more integers) and writing in memory By reading in order of the address which writes in the data written in the memory and is different from the time It is used in order to perform interleave processing which outputs the inputted data in different sequence from the sequence at the time of an input. It is the interleave address generation machine which generates read-out in said memory, and the address for writing. While performing count-up actuation from initial value 0 with the step size which synchronizes with a clock and is inputted from the exterior and outputting the counted value as read-out in said memory, and the address for writing When the counted value in the following clock timing becomes beyond the above ( $N \times M$ ) When it considers as the counted value in the following clock timing and further this counted value becomes ( $N \times M - 1$ ), the value which took the modulo of ( $N \times M - 1$ ) about the value The address count means constituted so that the counted value in the following clock timing might be returned to initial value 0, It is a means to calculate said step size and to output to said address count means. The value which took the modulo of ( $N \times M - 1$ ) about the value which multiplied the step size which is carrying out the current output by said  $M$  Set up as a new step size at the time of the interleave processing to the following block, and it synchronizes with the timing from which the counted value of said address count means returned to initial value 0. The interleave address generation machine characterized by having a step size operation means to change the step size outputted to said address count means into said set-up new step size.

[Claim 2] In an interleave address generation machine according to claim 1 said step size operation means While only said  $M$  batch carries out accumulation of the step size which is carrying out the current output during the period for [ until the counted value of said address count means is set to ( $N \times M - 1$ ) from initial value 0 ] 1 block A step size setting means to set up the value which took the modulo of ( $N \times M - 1$ ) about the accumulation value as a new step size at the time of the interleave processing to the following block, A detection means to detect that the counted value of said address count means became ( $N \times M - 1$ ), If it is detected that the counted value of said address count means became ( $N \times M - 1$ ) with this detection means, while memorizing the new step size set up with said step size setting means to the following clock timing The interleave address generation machine characterized by consisting of step size output means to output the memorized this step size to said address count means.

[Claim 3] In an interleave address generation machine according to claim 1 said step size operation means While performing the multiplication of the step size which is carrying out the current output, and said  $M$ , the value which took the modulo of ( $N \times M - 1$ ) about the multiplication value

Drawing selection **Representative drawing** 



[Translation done.]